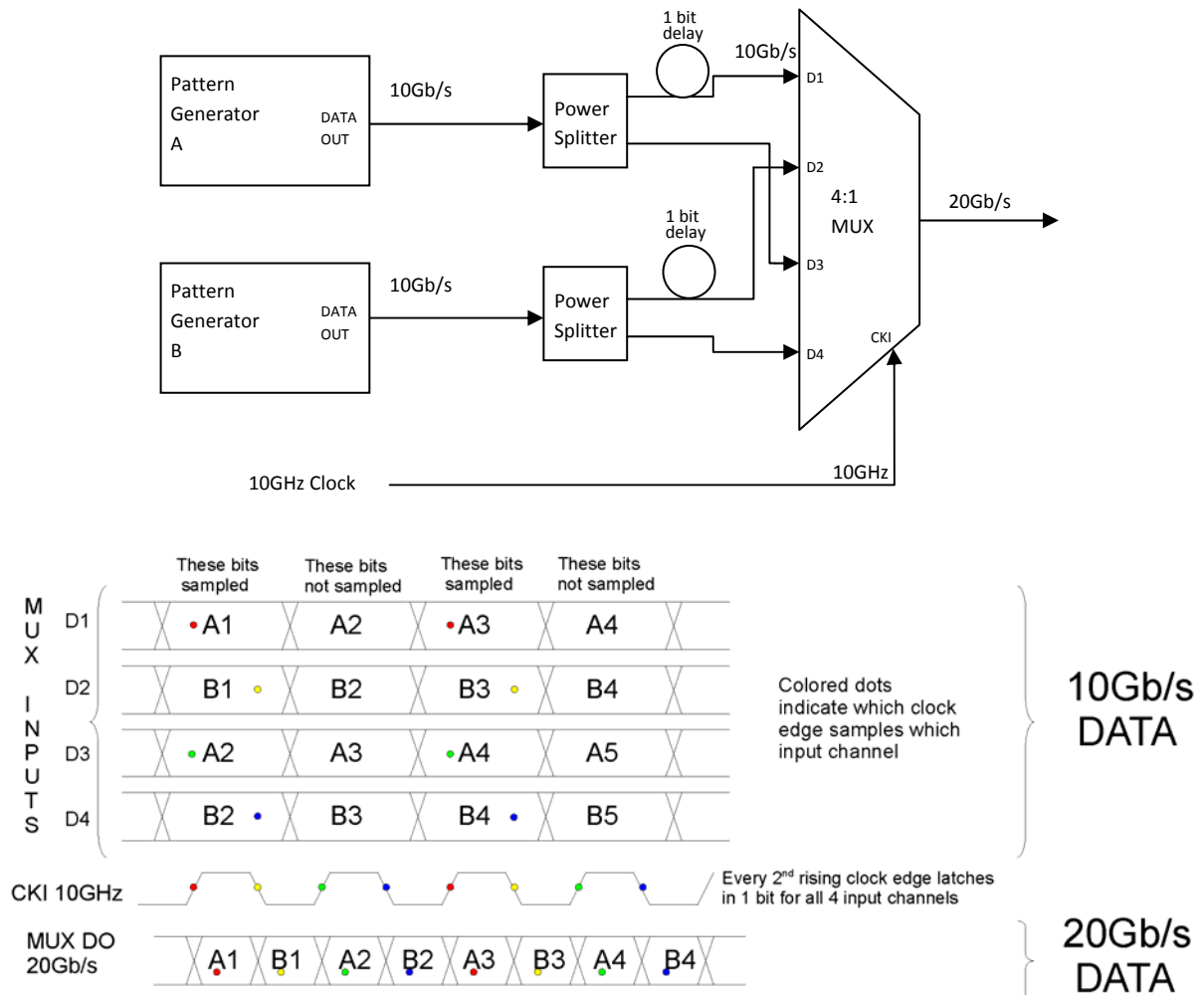


## AN25: How to use the Centellax MS4S1V1M and MS4S1V2M 4:1 Mux as a 2:1 Mux With a clock at the same rate as the input data.

1. With only 2 data signals to mux (A & B), you still need to make connections to all 4 data inputs of the mux. Take each data signal (A and B) and split each into two signals using a power splitter.
2. From the output of these final two splitters, connect to D1..D4 of the MUX as shown. One splitter output connects to D1 and D3. The other splitter output connects to D2 and D4. The connections to D1 and D2 must have an additional **1-bit** period delay over the connections to D3 and D4.
3. It is important to ensure that the all 4 signals arriving at the MUX inputs have the data eye crossovers exactly in phase with each other.
4. Apply a clock signal (at the same rate as the data inputs) to the clock input of the mux. (Note, in general the timing delay of the clock will need to be adjusted to ensure that the data inputs are sampled at the correct time. Timing is not shown in this example).
5. By making MUX Inputs D1=D3 and D2=D4, with the 1-bit delays included, the output of the 4:1 mux will be a data stream at 2x the data input rate.

### Example setup & timing diagram of a 2:1 mux with 2x 10Gb/s data inputs and 10GHz clock



## AN25: How to use the Centellax MS4S1V1M and MS4S1V2M 4:1 Mux as a 2:1 Mux

With a clock at the 2x the rate as the input data.

1. With only 2 data signals to mux (A & B), you still need to make connections to all 4 data inputs of the mux. Take each data signal (A and B) and split each into two signals using a power splitter.
2. From the output of these final two splitters, connect to D1..D4 of the MUX as shown. One splitter output connects to D1 and D2. The other splitter output connects to D3 and D4.
3. It is important to ensure that the all 4 signals arriving at the MUX inputs have the data eye crossovers exactly in phase with each other.
4. Apply a clock signal (at 2x the rate of the data inputs) to the clock input of the mux.  
(Note, in general the timing delay of the clock will need to be adjusted to ensure that the data inputs are sampled at the correct time. Timing is not shown in this example).
5. By making MUX Inputs D1=D2 and D3=D4, the output of the 4:1 mux will be a data stream at 2x the data input rate. (Actually the output is at 4x the input but every input bit is sampled twice).

Example setup & timing diagram of a 2:1 mux with 2x 10Gb/s data inputs and 20GHz clock

