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Characterizing Crosstalk Effects in High-Density High-Speed Backplanes

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Abstract

This document outlines the detrimental effects of crosstalk, discusses several methods of measuring crosstalk, and details the characterization of crosstalk in a high-density high-speed backplane.

BER-based jitter measurements are used to quantify the impairment caused by near-end crosstalk aggressors, far-end crosstalk aggressors, and automatically-swept phase relationships between aggressor channels and the victim channel.

Table of Contents

Crosstalk Defined

Crosstalk is the undesirable transfer of energy from data or clock signals to another part of the circuit or system. Crosstalk is an analog impairment caused by capacitive or inductive coupling of electromagnetic fields.

Dense high-speed signal routing in any complex 3D structure is vulnerable to crosstalk, which can cause the following signal integrity problems:

- Increased noise levels (decreased signal-to-noise ratio (SNR))
- Increased jitter on data edges (decreasing device margin over specifications)
- Reflections of undesired signals (reducing detector sensitivity)

Crosstalk effects can be mitigated by design changes. Increasing the physical separation of signal and clock lines, minimizing the distance traces run parallel to one another, interweaving ground isolation barriers, using multiple layers isolated with ground planes, and using differential signaling all reduce the amount of coupling. Unfortunately these design changes are limited by the desire for smaller devices with large numbers of data and clock lines.

Effective minimization of crosstalk requires an approach based on good layout design practices combined with engineering prototype characterization, and when necessary, ongoing production testing to ensure minimal changes due to manufacturing tolerances.

Simulating Crosstalk

Circuit simulation tools have recently made great strides in predicting circuit performance, but they are limited in their ability to predict the effects of crosstalk. The magnitude of crosstalk effects is determined by both the physical layout and electrical characteristics of devices, which can be very difficult to model correctly given the extreme ratio between the smallest modeled component and the overall size of the device.

Real-world devices often have multiple sources of crosstalk that further complicate simulation efforts. A multi-channel 10Gb/s switch circuit will suffer from crosstalk effects generated from many different components: the ASIC or circuit-level device, bondwires used to connect ICs to package substrates, the ceramic, plastic, or metalized package, and the PCB backplane connecting the packaged device to external connectors. Modeling each component separately is challenging, especially considering tolerances on manufacturing geometries, but modeling a complete device from connector to IC requires significant effort and considerable amounts of computational processing.

To further add to the complexity of modeling a complete device, consider that nearby aggressor channels generate uncorrelated signals that exponentially increase the complexity of electromagnetic field modeling. Crosstalk models featuring multiple independently-driven aggressors near both the victim channel input port and victim channel output port cannot currently be modeled by any commercially-available simulation software.

Measuring crosstalk is a key process step in manufacturing any high-speed high-performance device. Characterizing the worst-case performance of the device is necessary to ensure the design can support the desired channel density.

Measuring Crosstalk

Crosstalk can be characterized by several different methods, each of which uses a different instrument. The best method of measuring crosstalk depends on the desired format of the results (and also the test equipment available). Figure 1 summarizes the methods of measuring crosstalk.

Measurement	Domain	Pros	Cons
S-parameters (multi-port VNA)	Frequency	Can be used to identify package resonances; well-suited for characterizing analog circuit crosstalk	Crosstalk not stimulated by CW tones; multiple aggressors difficult to emulate; results unrelated to serial data metrics
Induced voltages (PG and scope)	Time	Can provide clues to crosstalk coupling location in device; can account for multiple aggressors	Doesn't account for phase relationship between aggressor and victim channel; results partially unrelated to serial data metrics
Total jitter (BERT)	Time	Measures aggressor impact on victim channel jitter; can account for multiple aggressors; accounts for phase relationships between aggressor and victim channels	Does not identify crosstalk coupling location

Figure 1 – Crosstalk measurement summary

Frequency-domain measurement of an induced signal

The classical approach to measuring crosstalk is to extract S-parameters from one channel while applying adjustable-frequency continuous wave (CW) stimulation to an aggressor channel. This measurement is made with a Vector Network Analyzer (VNA); the measurement generates S-parameters indicating the amplitude of energy coupled from an aggressor channel to the victim channel at many distinct frequencies.[viii]

The measurement methodology is the primary drawback of using S-parameters to measure crosstalk. Serial data systems are comprised of multiple channels of high-speed data, not multiple channels of CW frequencies. Crosstalk effects are not a CW phenomenon; crosstalk is the result of high-speed bit transitions occurring in the victim and aggressor channels. Crosstalk effects are magnified by fast data rise- and fall-times, which are not present in CW frequency tones.

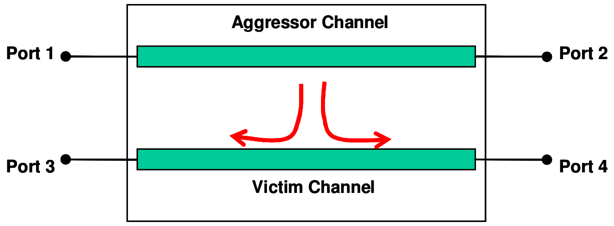


Figure 2 – S-parameter measurement setup

Figure 3 – 12-port VNA system[VIII]

As shown in Figure 2, a 4-port VNA system is required to measure the effect of one aggressor channel. Stimulating multiple aggressor channels requires twice the number of ports on the VNA, and aggressor channels can only be swept independently.[viii]

A second disadvantage to using S-parameter measurements to quantify crosstalk is correlating the measurement results to crosstalk effects. Figure 4 shows measurement data collected from a multi-port VNA. The data shows that static CW crosstalk between one aggressor and the victim channel ranges from -70 to -30dB over the frequency range, but this result is difficult to interpret in terms of eye closure, increased bit error rate, or other metrics relevant to a serial data system.

The open-source program StatEye, developed during OIF CEI development, can import S-parameters and be used to estimate the impact of crosstalk on a victim channel, but the results provided are calculated, not measured, and as such are strongly determined by the setup and configuration of the StatEye program. Centellax strongly recommends comparing simulated calculations against measurements!

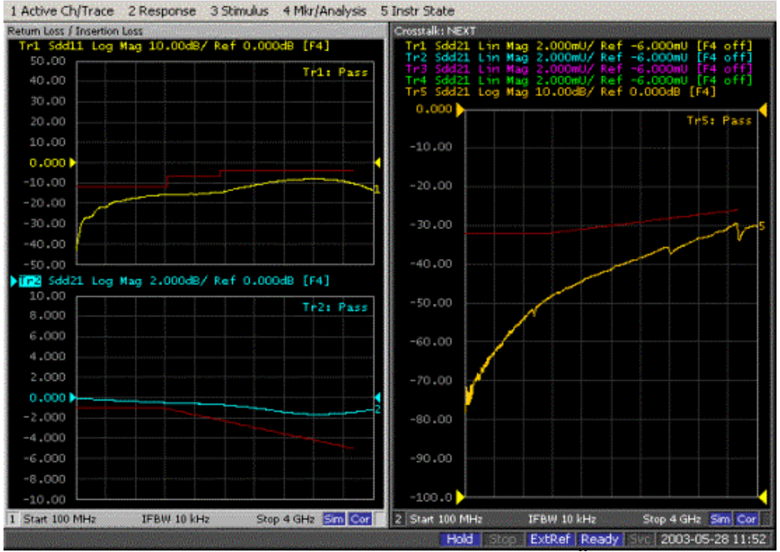
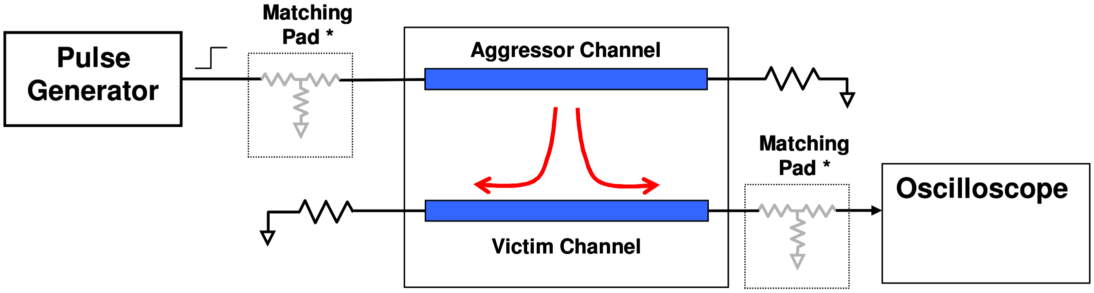


Figure 4 – S-parameter measurement results[vii]

Time-domain measurement of an induced signal

The second method of measuring crosstalk uses a pattern generator to stimulate an aggressor channel while an oscilloscope captures the shape of the induced signal on the victim channel, as shown in Figure 5.



* Impedance matching networks are used if Agressor or Victim channels are not 50 Ω

Figure 5 – Time-domain induced signal measurement setup

The oscilloscope measures crosstalk by capturing the time-varying voltage induced on the victim channel by the signal on the aggressor channel. Figure 6 illustrates the victim-channel voltage pulse (shown in red) created by a fast data transition on the aggressor channel (shown in yellow), as captured by a Tektronix scope (detailed in reference ix). Similar to S-parameter measurements, this measurement result is difficult to relate to the effect on data integrity in a serial data system.

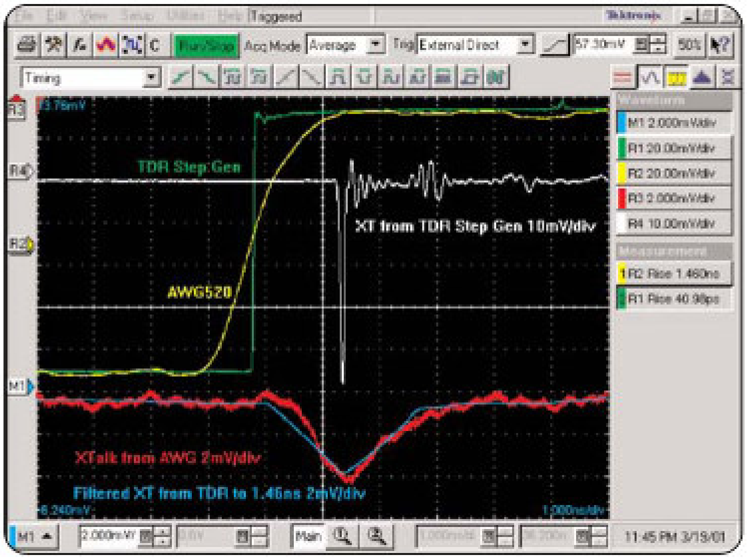


Figure 6 – Time-domain induced signal measurement results[ix]

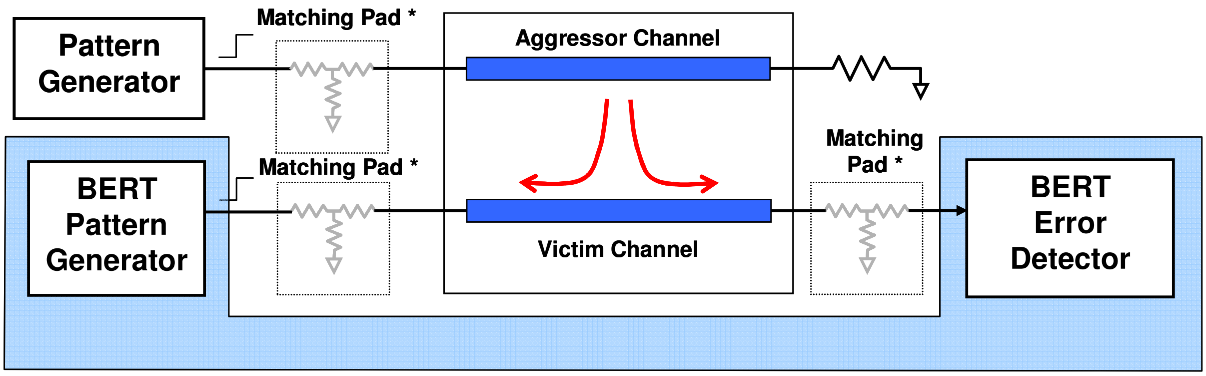
The missing link is the time dependence of the aggressor signal transition relative to the victim channel. In a serial data link, the victim channel is only susceptible to bit errors induced by crosstalk if the aggressor signal alters victim waveshape during the time window where the receiver samples the data. The 4mV crosstalk pulse shown above would have no effect if it impacts the victim channel at a non-consequential location. Without considering the impact of crosstalk on a data bitstream on the victim channel, this method cannot predict how the victim channel will perform when impaired.

Another important note to consider when using this measurement technique is to ensure that all aggressor channels are simultaneously stimulated. The effects of one aggressor may be limited to a 4mV pulse, but the effects of multiple aggressors will combine together and create larger discontinuities on the victim channel. This is discussed further in the next section.

Time-domain measurement of victim channel jitter

The third method of measuring crosstalk examines the metric most important to serial data systems: the width of the eye opening. A larger eye opening means lower BER measurements and a larger margin to account for manufacturing tolerances and transmission channel losses. Eye opening width is characterized by measuring the total jitter (TJ) of the victim channel.

This measurement method is enhanced by loading both aggressor channels and the victim channel with pseudo-random bit sequence (PRBS) patterns, shown in Figure 7. This enables a comparison of TJ measurements both with and without aggressors, which yields a direct measurement of victim channel signal degradation caused by crosstalk.



* Impedance matching networks are used if Agressor or Victim channels are not 50 Ω

Figure 7 – Time-domain jitter measurement setup

TJ measurements must be made at the appropriate BER level – most specifications call for TJ measured at 1E-12 BER depth – and at an acceptable confidence interval. Figure 8 shows a TJ measurement at 1E-9 and a TJ extrapolation at 1E-12. Making BER-based TJ measurements is discussed in Centellax appnote AN23, "BER-Based Jitter Measurements".[xiii]

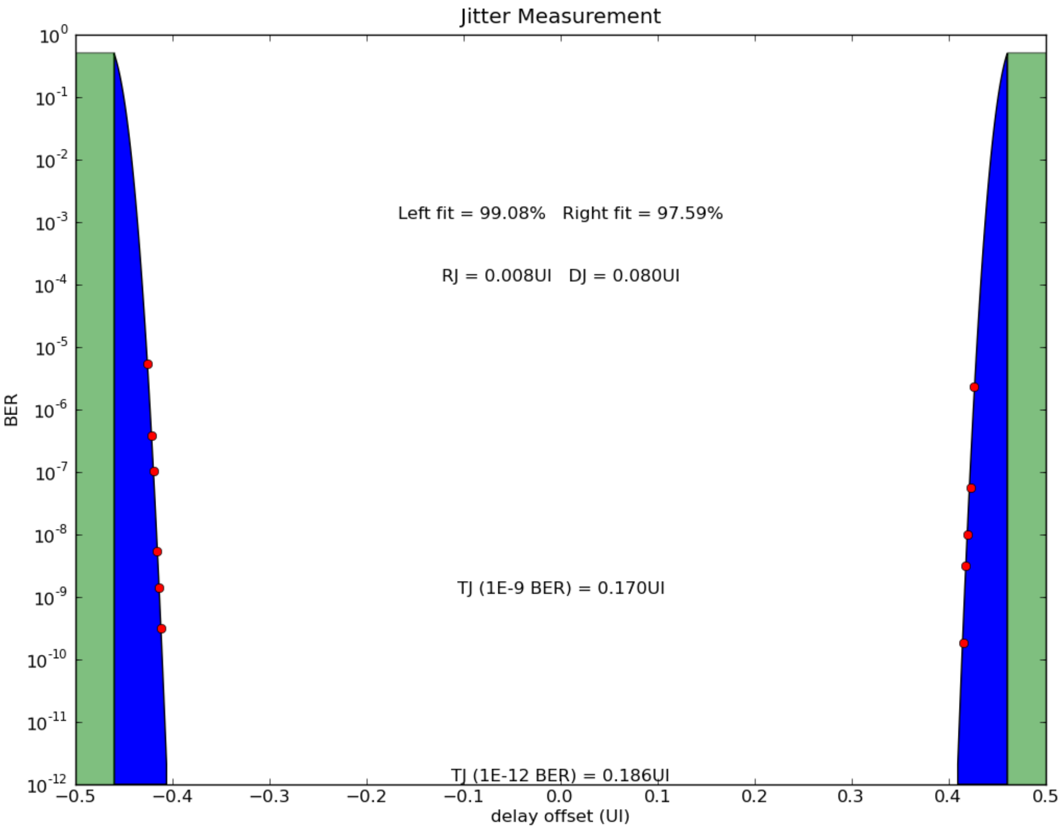


Figure 8 – BER-based jitter measurement: 8Gb/s, PRBS7, 1V amplitude, 0dB de-emphasis, DUT: short differential cable

Centellax recommends using a BER tester to measure TJ to 1E-10 BER depth with >99.5% CI and extrapolating to 1E-12 BER only when Q-scale fit values are greater than 95%. BER testers sample every bit, can be used with long PRBS patterns, and are widely accepted as the best instrument for measuring TJ.[x,xi,xii]

As noted above, all aggressor channels and the victim channel must be simultaneously stimulated with PRBS patterns to accurately characterize the effects of crosstalk. Crosstalk impairments constructively combine together, so measurements that consider only some of the neighboring signal lines as aggressors will understate the victim channel susceptibility.

The type of pattern used on victim and aggressor channels is also important. We strongly recommend using uniquely-generated and randomly offset full-rate PRBS patterns of different lengths. Fast pattern rise- and fall-times are directly related to the efficiency of electromagnetic coupling, so using slower-speed aggressor signals or auxiliary clocks (meant to approximate a 1010 bit sequence) is ineffective. PRBS7 patterns are often used to emulate the short repeating pattern length associated with encoded data, while PRBS31 patterns are used due to the long sequences of ones and zeros in the pattern. These long sequences generate the lowest frequency tones present in any data pattern.

Equally important in measuring the impact of crosstalk is the phase relationship between aggressor channels and the victim channel. As noted in the previous section, aggressor channel transitions will induce transient waveforms on the victim channel. The position of these waveforms is critically important to the impact they have on the measured jitter. If all aggressors are aligned such that induced victim-channel transients fall in the unimportant transition zone, the jitter performance of the victim channel may not be affected. Aggressor channels must be either independently clocked or independently skewed while jitter measurements are underway. The Centellax PCB12500 has an automatic channel delay sweep mode that is ideally suited for this purpose.

For best approximation of the random data relationship found in serial data connections:

- Victim channel and all neighboring aggressor channels should be loaded with independent full-rate PRBS data
    - Connect signals differentially or single-ended to reflect how the DUT will be used; differential connections will be less susceptible to crosstalk
    - Terminate other ends of aggressor channels in 50ohm loads (unterminated channels will reflect signals back into the device, which may cause more crosstalk but is unlikely to reflect the DUT use condition)
- PRBS patterns must be used
    - Pattern risetime is directly related to effectiveness of crosstalk, so using an auxiliary clock to approximate a 1010 bit sequence is ineffective
    - PRBS7 patterns emulate short pattern length of encoded data

  - PRBS31 patterns contain long sequences of zeros and ones; these generate the lowest frequency tones in the pattern spectral density
- Unsynchronized aggressors
  - Phase relationship of bit transitions is critical for crosstalk coupling
  - Clock all aggressors and victim channel pattern generators independently, or sweep delay phase while making measurements
  - Ensure patterns are offset by random amounts; do not use one pattern generator and power-split outputs for multiple channels: the phase relationships will be fixed and bit sequences will be similar
- Victim channel and aggressor channels must have appropriate configuration
  - Victim and aggressor channel signal amplitude, offset, crossover, and jitter must represent the signal configuration in the use case

Characterizing AdvancedTCA Backplane Crosstalk

The following section details the characterization of an AdvancedTCA backplane, a board designed for the next generation of "carrier grade" communications equipment. The backplane provides point-to-point connections between cards inserted in specific slots; it does not use a data bus.[xiv] Figure 9 shows the DUT and measurement equipment discussed in this section.

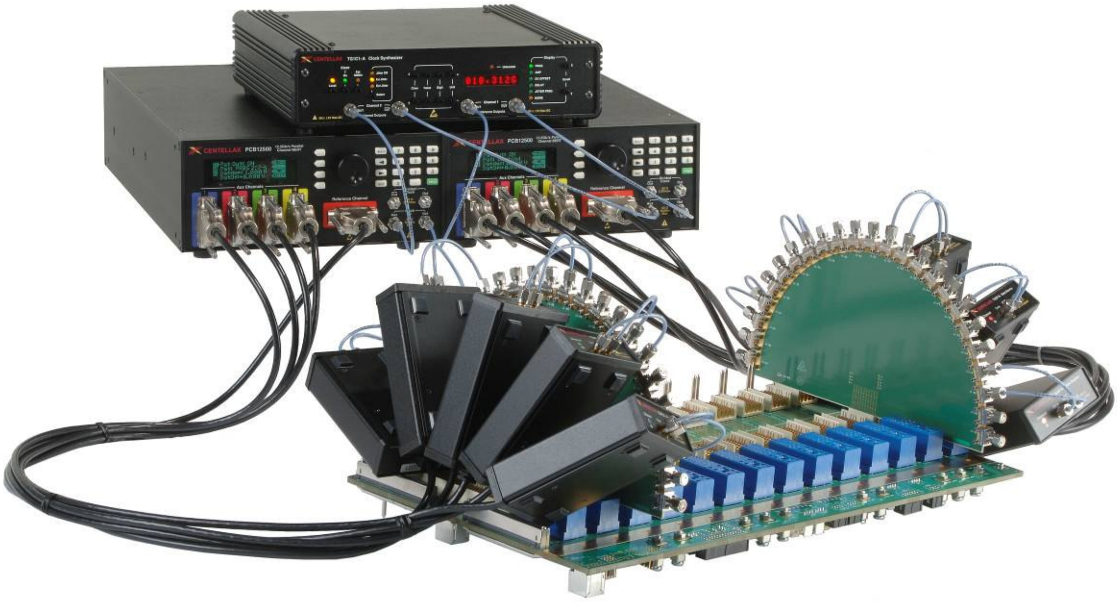


Figure 9 – AdvancedTCA backplane with two probe cards, connected to nine Centellax TG5P1A Pattern Generator heads, one TR2P1A Error Detector head, two PCB12500 Parallel Channel BERTs, and one TG1C1-A Clock Synthesizer

Backplane and Test Configuration

The backplane we are testing is compliant to PICMG 3.0, a Fabric-agnostic specification that can be used with Ethernet, Fibre Channel, StarFabric, PCI Express, and RapidIO. The backplane is configured in a manner that connects 15 channels on Logical Slots 1 & 2 to the 12 other node slots. Figure 10 shows the channel configuration on the fabric interface.

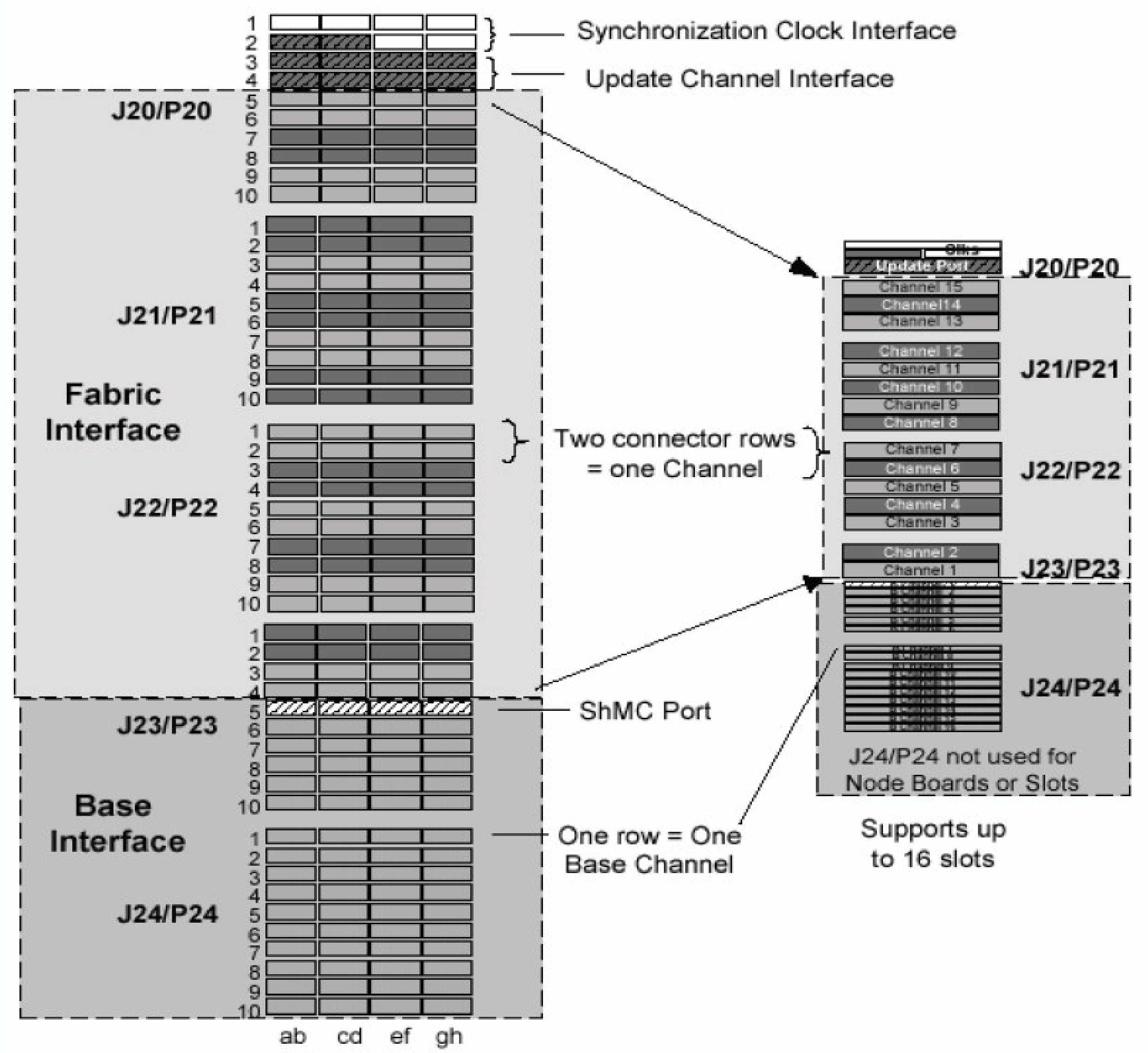


Figure 10 – Fabric interface to the AdvancedTCA backplane[xv]

To test the longest channel length on the backplane, which includes short via stub discontinuities, the probe cards are connected from fabric channel 13 (logical slot 1, rows 9 and 10) to fabric channel 1 (logical slot 14, rows 3 and 4) as shown in Figure 11.

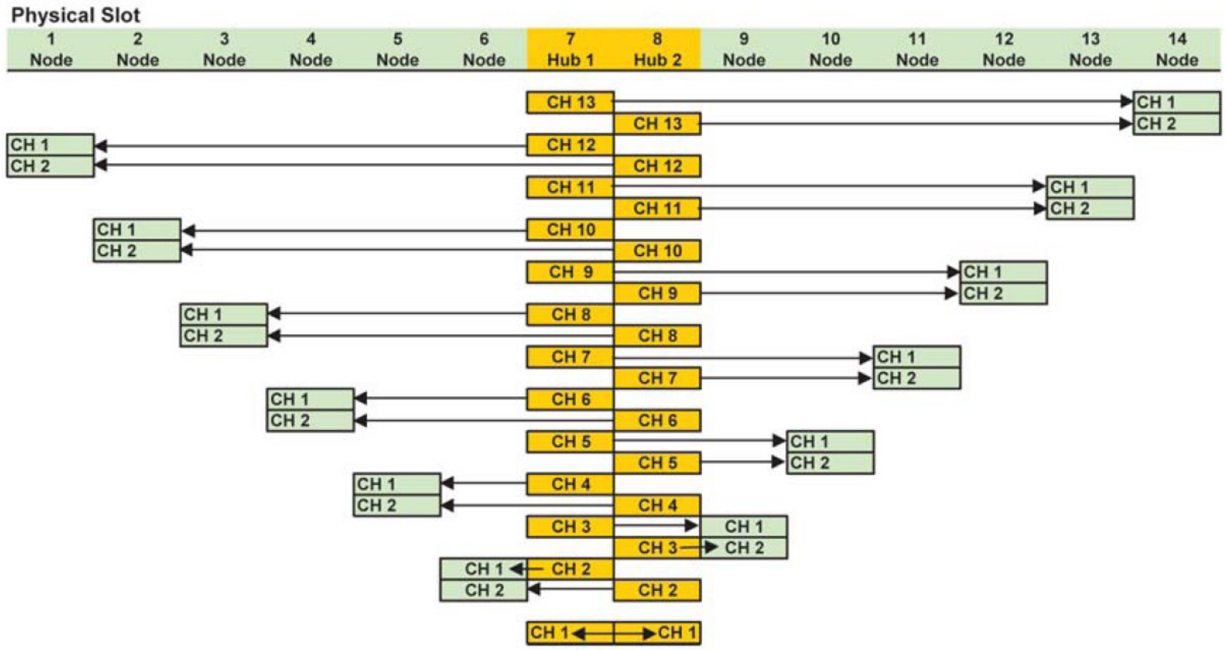


Figure 11 – DUT backplane routing diagram

High-speed signals interface with the AdvancedTCA backplane through ZD connectors, which connect five rows of four differential signal pairs per row. The probe cards connected to the backplane break out three rows of signals. These 12 differential signals (24 connectors) then interface to the test instruments with short flexible SMA connectors. The role assignment diagram is shown in Figure 12.

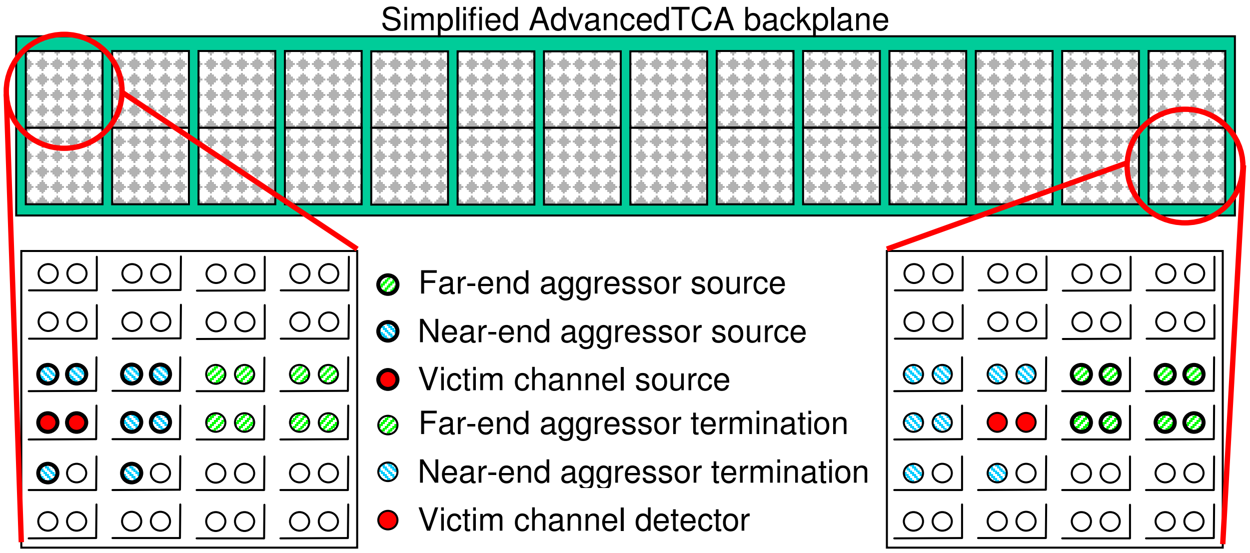


Figure 12 – Backplane channel victim / aggressor role assignment

Test Instruments (PCB12500)

The Centellax test instruments used in the characterization of the AdvancedTCA backplane are:

- TG1C1-A Clock Synthesizer (provides clocks to PCB12500s)
- PCB12500 Parallel Channel BERT (controls remote heads)
    - TG5P1A Pattern Generator head (victim channel generator)
    - Four TG5P1A Pattern Generator heads (near-end aggressors)
- PCB12500 Parallel Channel BERT (controls remote heads)
    - TR2P1A Error Detector head (victim channel detector)
    - Four TG5P1A Pattern Generator heads (far-end aggressors)

The PCB12500 Parallel Channel BERT is an ideal instrument for characterizing multi-channel crosstalk with multiple aggressors. In this case we decided to use two PCB12500 controllers to stimulate both near-end and far-end aggressors. The victim generator, victim detector, and all but two aggressor generators were connected with differential phase-matched cables as shown in Figure 12.

The PCB12500 controller supports up to 5 remote heads. We are using two different types of heads: TG5P1A Pattern Generator heads (with de-emphasis), and TR2P1A Error Detector heads. The PCB12500 controls each head and provides each with an independently-controlled phase-shifted clock.

The TG5P1A Pattern Generator head has full PRBS pattern adjustability, amplitude control, offset adjustment, crossover adjustment, delay offset adjustment, and most important for this application: fully integrated de-emphasis capability, which is required for high-speed signal transmission through the AdvancedTCA backplane. During pre-characterization analysis with the backplane we determined that 4.0dB de-emphasis was optimal; this was used for all measurements. Non-emphasized signals could not be characterized due to backplane losses.

The TR2P1A Error Detector head has full PRBS pattern adjustability, zero/one sampling threshold adjustment, delay offset adjustment, and full delay and amplitude centering capability.

The PCB12500 has a key feature for use in high-density crosstalk applications: automatic delay sweeping. This feature sweeps the delay offset on any channel in a triangle wave of 1UI, 2UI, or 4UI range. Each channel is swept at a different frequency and all frequencies are prime numbers. The channel, sweep frequency, delay step size, and time between steps are summarized in Figure 13.

Channel	**Freq**	**1UI Step Size; Time between steps**	**2UI Step Size; Time between steps**	**4UI Step Size; Time between steps**
0	7Hz	20mUI; 1.429mS	40mUI; 2.857mS	80mUI; 5.714mS

1	11Hz	20mUI; 0.909mS	40mUI; 1.818mS	80mUI; 3.616mS
2	13Hz	20mUI; 0.769mS	40mUI; 1.538mS	80mUI; 3.077mS
3	17Hz	20mUI; 0.588mS	40mUI; 1.176mS	80mUI; 2.353mS
4	19Hz	20mUI; 0.526mS	40mUI; 1.053mS	80mUI; 2.105mS

Figure 13 – PCB12500 Parallel Channel BERT delay sweep summary

The automatic delay sweep functionality enables each of the aggressor channels to be independently adjusted relative to the un-swept victim channels. This offers the ideal situation where the bit transitions on every aggressor channel are moved to every possible phase relationship to the bit transition of the victim channel. While longer gate times are required to account for the thousands of different phase relationships possible with multiple aggressors, this feature guarantees that the most stressful phase relationship between victim and aggressor channels is tested.

Measurement Results

Figure 14, Figure 15, and Figure 16 are measurement results from prototype Centellax Test Solutions software. The graphs show BER measurements as red points, the blue RJ section of the eye (with fitted curve based on a linear Q-scale curve fit; least-square fit metrics annotated), and green sections illustrating the DJ portion of the eye. The TJ measurement at 1E-9 and TJ estimation at 1E-12 BER depths are shown.

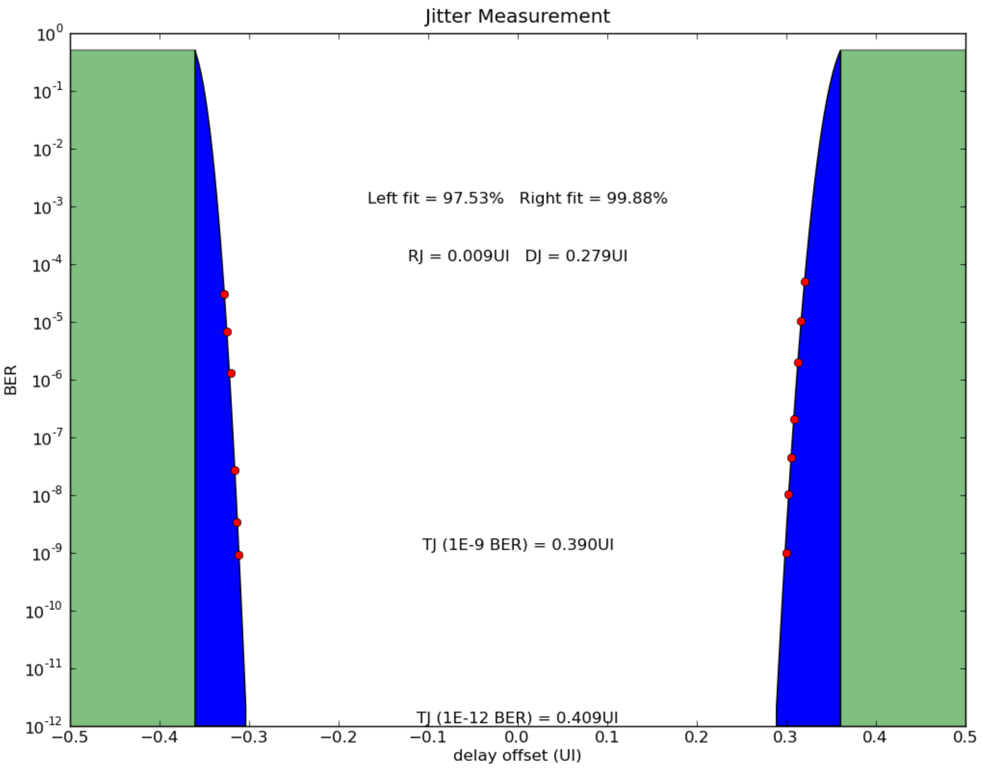


Figure 14 – AdvancedTCA backplane at 8Gb/s; PRBS7, 2V amplitude; no aggressors

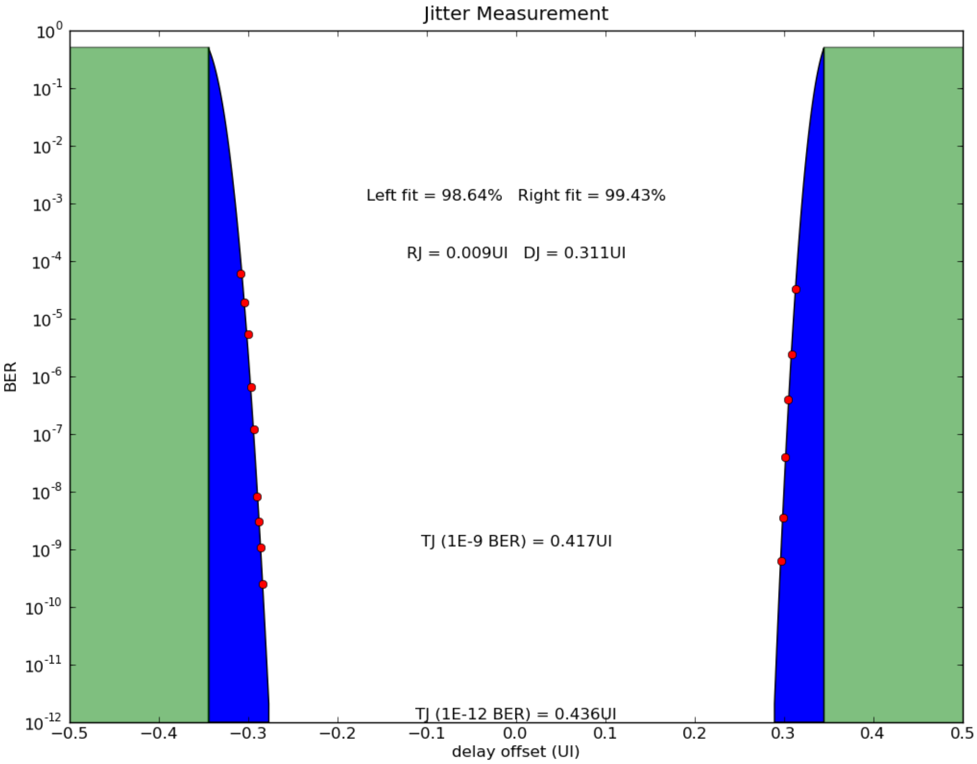


Figure 15 – AdvancedTCA backplane at 8Gb/s; all channels: PRBS7, 2V amplitude; Near-end aggressors without delay sweep; Far-end aggressors without delay sweep

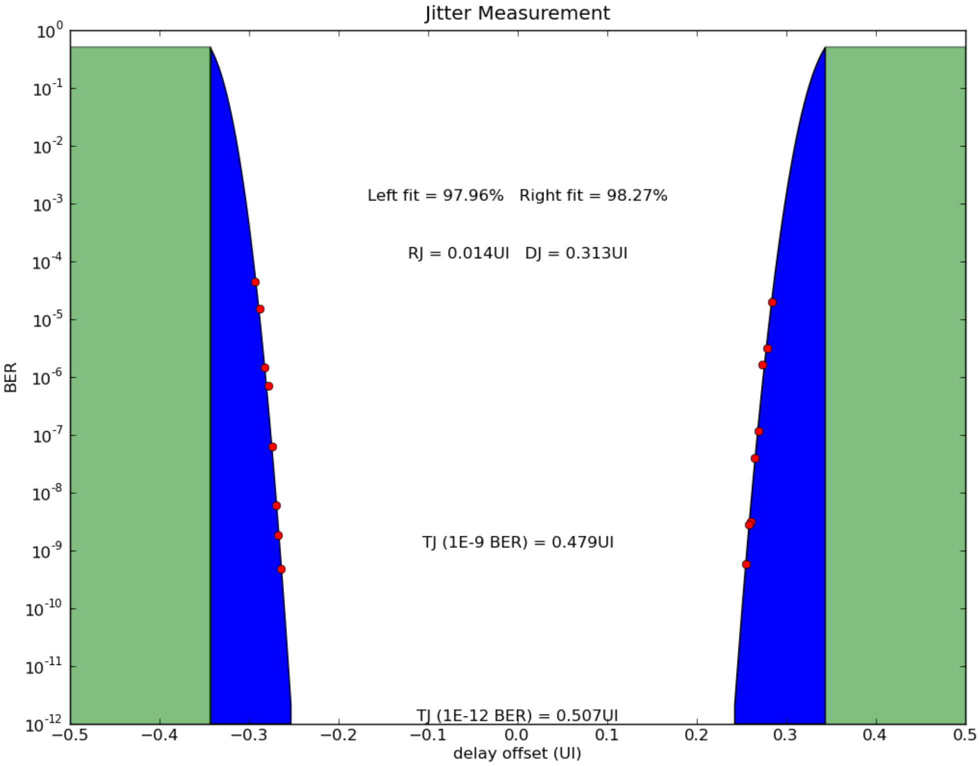


Figure 16 – AdvancedTCA backplane at 8Gb/s; all channels: PRBS7, 2V amplitude; Near-end aggressors with delay sweep; Far-end aggressors with delay sweep

The measurement results summarized in Figure 17 show that this test configuration is most sensitive to near-end aggressors and less so to far-end aggressors. This is probably due to the aggressor signal configuration (physical proximity) in relation to the victim channel, as shown in Figure 12.

PRBS7	TJ (1E-9 BER)	TJ (1E-12 BER)	DJ	RJ
No aggressors	0.390UI	0.409UI	0.279UI	9mUI
Near-end aggressors	0.419UI	0.437UI	0.313UI	9mUI
Far-end aggressors	0.403UI	0.421UI	0.295UI	9mUI
Near- and far-end aggressors	0.417UI	0.436UI	0.311UI	9mUI
Near- and far-end aggressors with delay sweep	0.479UI	0.507UI	0.313UI	14mUI

Figure 17 – Jitter measurements of AdvancedTCA backplane at 8Gb/s

The results also highlight the importance of the delay sweep feature of the PCB12500 Parallel Channel BERT. Without delay sweep the delay relationship between both the near- and far-end aggressor channel transitions and the victim channel transitions is static. The voltage wave each aggressor induces on the victim channel, similar to the waveform shown in Figure 6, is induced at some random location in the victim channel eye. The impact of each aggressor channel is averaged over the victim channel.

The delay sweep feature ensures that all possible variations of the relationship between aggressor channel transition and victim channel transition occur while making each BER measurement. As shown in the results this feature finds the 'worst-case' scenario, which is an effective increase in the accuracy of the jitter measurement. The delay sweep feature enables better characterization of the device under test.

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