AN11: Application block diagrams for 10G BERT test systems

Centellax designs and manufactures a collection of low-cost instruments and test accessories, including a 10G BERT for 0.5-12.5Gbps applications. The TG1B1-A can be used for a collection of signal integrity applications as listed below:

1. Pattern generator for use with oscilloscope
2. BER tester for use with a simple electrical DUT for 10G applications
3. BER tester with an external 1/16th rate clock for 10G applications
4. BER tester with an external divider for low-rate applications
5. BER tester with an external full-rate clock for 0.5-12G applications
6. BER tester with jitter injection for stressed eye testing
7. BER tester with Centellax TR1C1-A Clock Recovery Unit

Each application is discussed in detail with block diagrams below. For more information, please contact support@centellax.com.

Pattern generator for use with oscilloscope

The TG1B1-A can be used as a high-performance GPIB-programmable PRBS (pseudo-random bit sequence) generator. This application is ideally suited for measuring the eye performance of the DUT, including 'eye mask' measurements.

A simple PRBS generator block diagram is shown in Figure 1; this setup is used to characterize the output performance of the BERT. The two small coaxial loops are shown connecting the BERT clock outputs to the clock inputs. The LF TrigO (615-709MHz) output is connected to the scope trigger input.

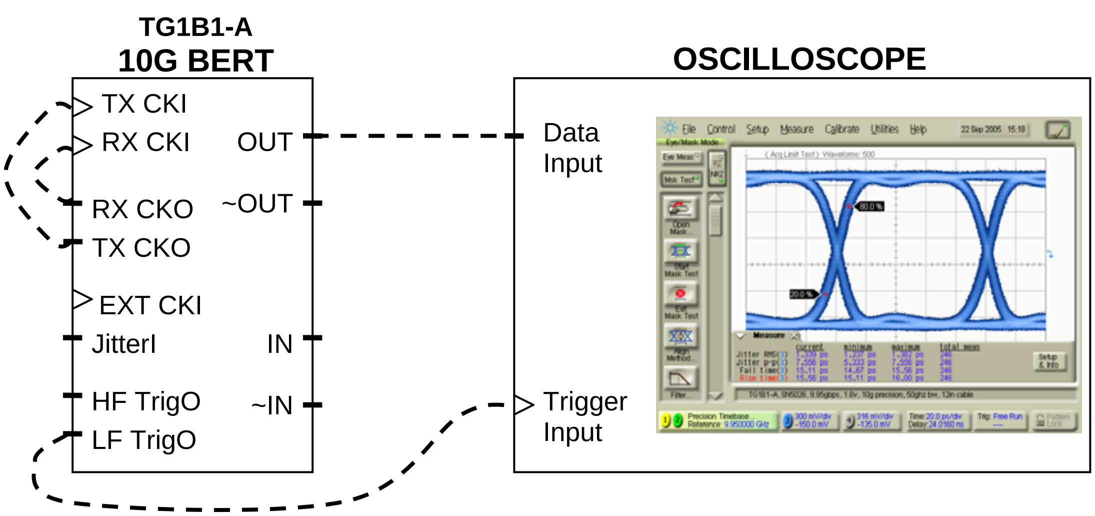

Figure 1 – block diagram – performance verification with oscilloscope

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Once the BERT output has been characterized with rise/fall times, RMS and p-p jitter, output amplitude, eye height, signal-to-noise ratio, etc, a common application is to measure the performance of a DUT, shown in Figure 2.

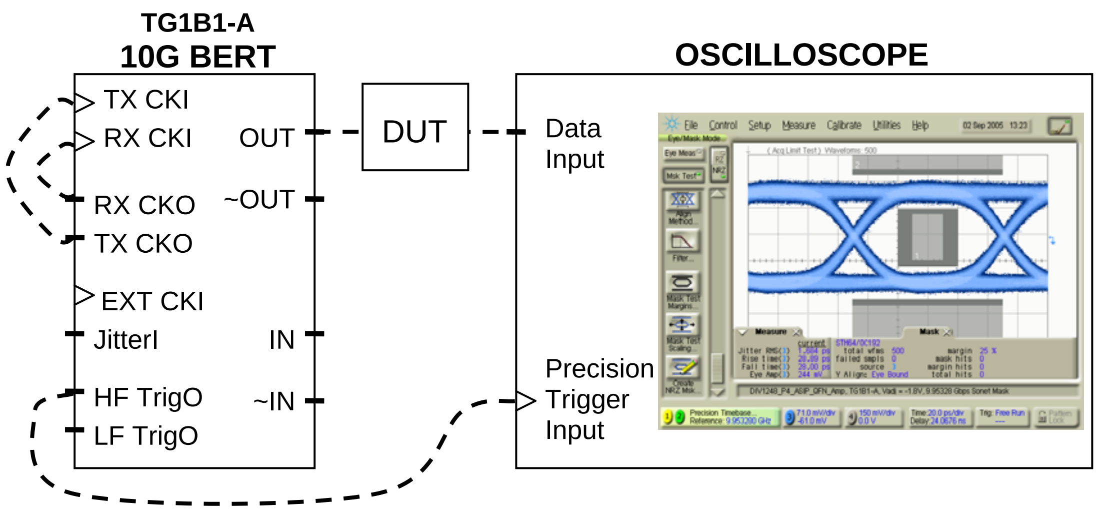

Figure 2 – block diagram – DUT eye-mask measurement with oscilloscope

In this case, we are using the 'precision timebase', a high-precision trigger input on the oscilloscope. This scope input can accept a higher frequency rate trigger signal, and is connected to HF TrigO (a full-rate clock) on the BERT.

Even though we are using a more precise method of triggering the oscilloscope, the performance of the DUT is slowing down the transition times and increasing RMS jitter. The scope is shown making an 'eye-mask' measurement.

BER tester for use with a simple electrical DUT for 10G applications

The TG1B1-A can be used as a high-performance GPIB-programmable BERT (bit error rate tester). This application is ideally suited for measuring the errors caused by an electrical DUT operating at 10G (9.85-11.35Gbps, to be exact).

A block diagram is shown in Figure 3; this setup is used to verify the performance of the BERT. By connecting the OUT directly to the IN, the BERT will measure the amount of signal degradation introduced by the coaxial cable – this should result in BER=0 at most phase adjustment settings.

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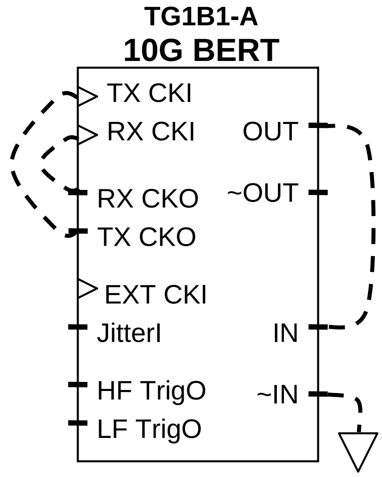

Figure 3 – block diagram – BERT verification measurement

Another block diagram is shown in Figure 4; this setup is used to measure the BER introduced by a simple single-ended electrical DUT. The two cables used to connect the DUT to the output and input do not need to be phase-matched.

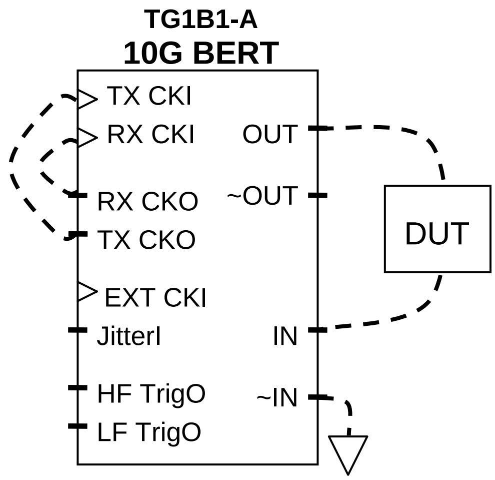

Figure 4 – block diagram – BER measurement of single-ended DUT

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BER tester with an external 1/16th rate clock for 10G applications

The TG1B1-A can also be synchronized to an external 1/16th rate clock for BER measurements from 9.85 to 11.35Gbps. This application is ideally suited for synchronizing the BERT with the system clock of a DUT, like a transceiver, SERDES, or CDR.

A block diagram is shown in Figure 5. The external low-frequency (LF, clock/16) signal is connected to ExtCKI. The BERT ***synth*** option should be changed to 0, and the ***freq*** option to the approximate frequency rate (clk/16 * 16).

Note: The clock signal applied to the ExtCKI port must be within the range of 615-709MHz; this signal is multiplied by 16 and output from the TX CKO and RX CKO outputs. Frequencies outside this range will not be correctly multiplied by the BERT internal clock system.

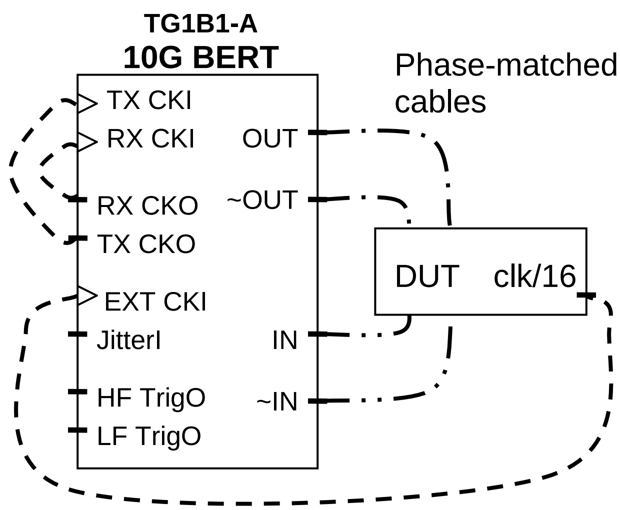

Figure 5 – block diagram – BER measurement of DUT synchronized with 1/16th rate clock

Note: To ensure the phase lock of an external LF clock applied to the ExtCKI port, reference the procedure detailed in Section 2.2 of the Users' Guide.

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BER tester with an external divider for low-rate applications

The TG1B1-A can also be used for applications below the internal clock range of 9.85 to 11.35Gbps, within the operating limits of 0.5-12.5Gbps. This is accomplished by using an external divider (Centellax offers several programmable units) in the clock path, as illustrated in Figure 6.

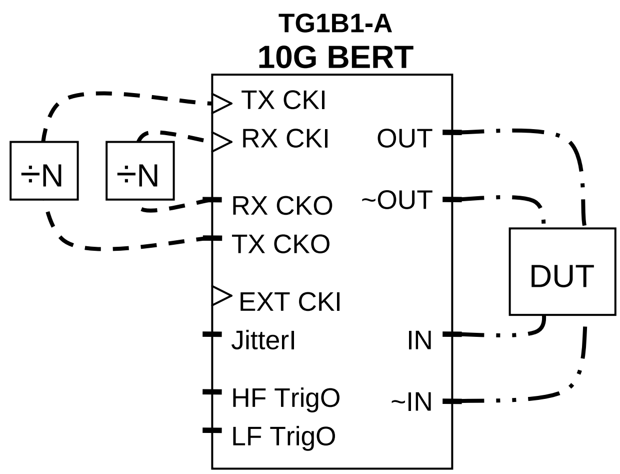

Figure 6 – block diagram – BER measurement of low operating rate differential DUT

The output from the BERT internal clock system (RX CKO and TX CKO) is GPIB and front-panel programmable between 9.85-11.35GHz. Using external dividers, part number UXC20PE, the clock can be divided to a lower rate and the test system can be used in the operating ranges listed in Table 1.

Because the BERT receiver has an internal electronic phase-adjuster, the coax cables connecting the TX CKO and RX CKO to the dividers, and the dividers to the TX CKI and RX CKI inputs, do not need to be phase matched.

Table 1 – BERT operating range with external programmable divider

Divider	Divide Ratio	Operating Range
None	None	9.85-11.35
UXC20PE	Divide-by-2	4.925-5.675
UXC20PE	Divide-by-4	2.4625-2.8375
UXC20PE	Divide-by-8	1.23125-1.41875

Consult the BERT Users' Guide for detailed procedures regarding the use of an external clock: change the ***synth*** option to 0, then adjust the ***freq*** setting.

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BER tester with an external full-rate clock for 0.5-12.5G applications

The TG1B1-A can also be used for applications within a full range of operating rates from 500Mbps to 12.5Gbps. This is accomplished by applying an external clock signal to the BERT clock inputs, RX CKI and TX CKI, as illustrated in Figure 7.

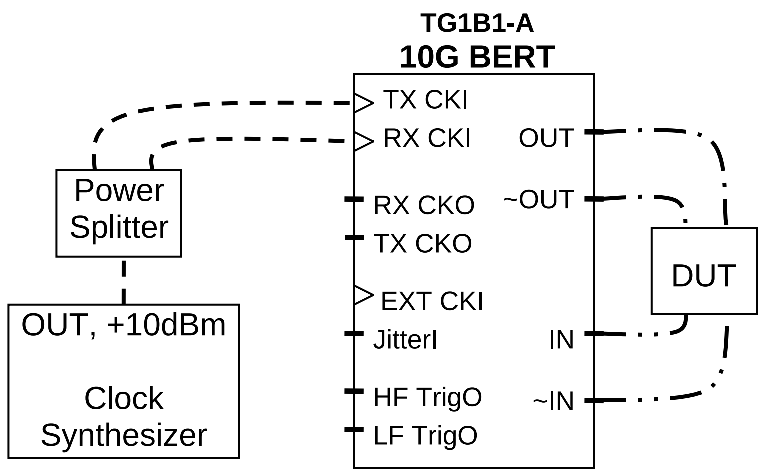

Figure 7 – block diagram – multi-rate BER measurement of DUT with external clock

Because the BERT receiver has an internal electronic phase-adjuster, the coax cables connecting the power splitter to the TX CKI and RX CKI inputs do not need to be phase matched.

The clock input (TX CKI and RX CKI) power input requirements are typically +4dBm, so the synthesizer should generate more than a +7dBm output if a power splitter is used.

Consult the BERT Users' Guide for detailed procedures regarding the use of an external clock: change the ***synth*** option to 0, adjust the ***freq*** setting to the approximate frequency rate.

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BER tester with jitter injection for stressed eye testing

The TG1B1-A also has the capability to inject jitter onto the output PRBS datastream; an important component of IEEE-specified stressed eye tests. This is accomplished by applying an external signal to the JitterI input port as illustrated in Figure 8.

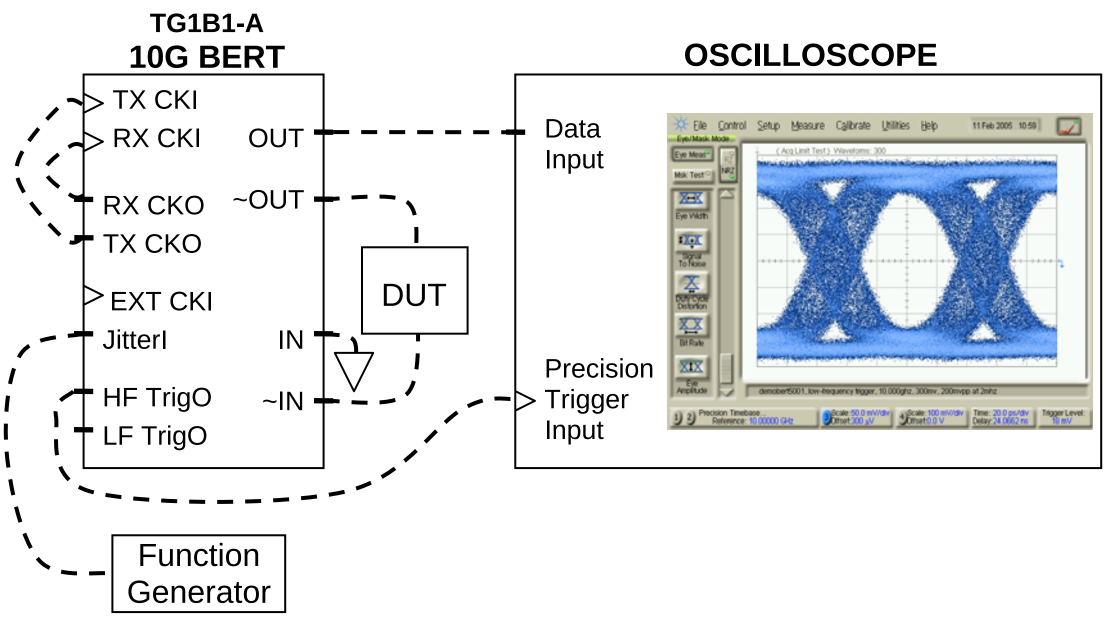

Figure 8 – block diagram – BER measurement with jitter injection for stressed eye testing

The function generator generates the signal that the BERT FM modulates onto the full-rate clock. This is typically a sinusoid, but the JitterI input could be a square wave, a Gaussian noise source, and even an uncorrelated PRBS bit stream.

The JitterI input bandwidth is DC-100MHz; the TG1B1-A Users' Guide spells out the amount of UI that can be injected in Section 2.2. The UI injection vector is also supplied, relating the input voltage to UI of jitter injected.

The jitter is applied to the TX CKO and HF TrigO outputs. The RX CKO and LF TrigO outputs are not jittered. The JitterI input requirements range from 0 to 2V.

Consult the BERT Users' Guide for detailed procedures regarding the use of the jitter injection feature: change the ***jitter*** option to 1.

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BER tester with Centellax TR1C1-A Clock Recovery Unit

The TG1B1-A can also be used with a broadband clock recovery unit, like the low-cost Centellax TR1C1-A. This "AnyRate" CRU will recover a clock from a PRBS bitstream from 622Mbps to 13.5Gbps – perfect for use with the wide operating range of the Centellax BERT. By recovering the clock from the DUT output, the BERT can accommodate tests where polarization mode dispersion (or other physical effects) can change the period of the data. This is illustrated in Figure 9.

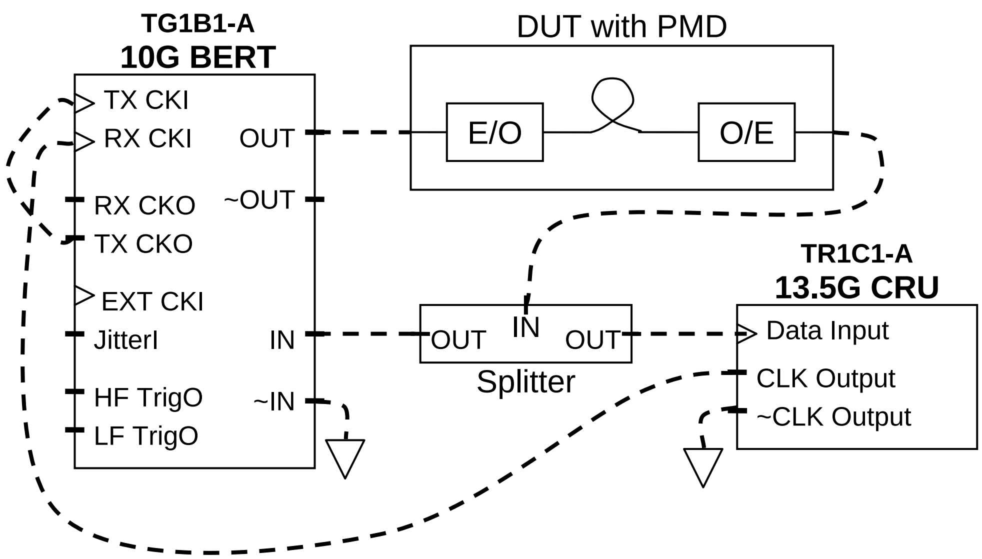

Figure 9 – block diagram – BER measurement with Centellax Clock Recovery Unit

A passive power splitter is required to duplicate the output signal of the DUT to feed the BERT and CRU input. If the output from the DUT is severely degraded or very low in amplitude, a buffer or retiming stage may be required to boost the amplitude to meet the sensitivity of the BERT and CRU.

If the DUT has a differential output, one side should be delivered to the BERT IN, and the other side should be connected to the CRU input. This will eliminate the power splitter from the block diagram, and will allow operation at lower DUT output levels. This is shown in Figure 10.

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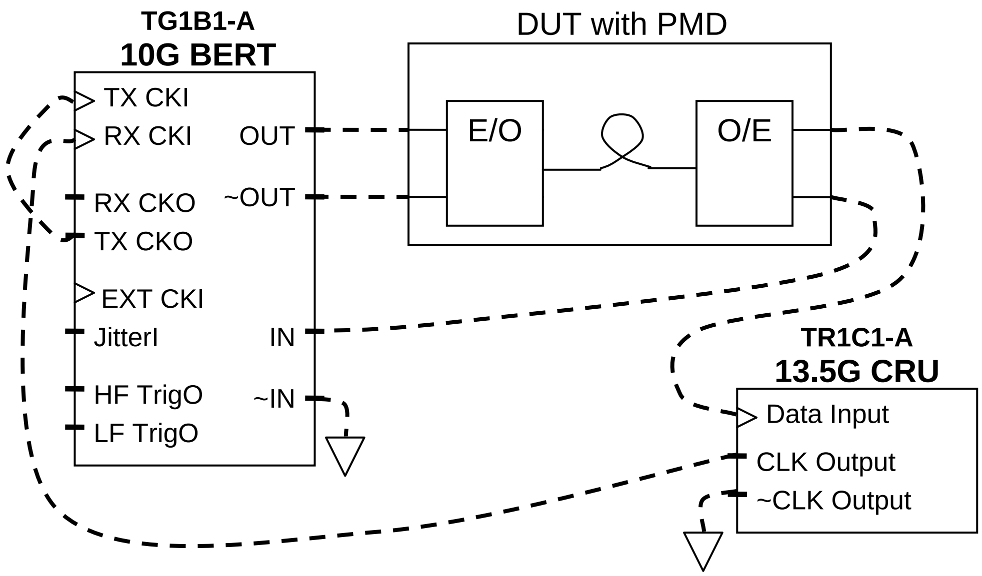

Figure 10 – block diagram – Differential BER measurement with Centellax CRU

The TR1C1-A will automatically scan between 622Mbps and 13.5Gbps, and will lock onto the highest-power frequency rate it can find. The recovered clock is ideally suited to drive the BERT error detector.

Consult the CRU Users' Guide for detailed procedures regarding the use of the clock recovery unit.