

AN10: Programmable divider system for 10g BERT test system

Abstract

The TG1B1-A operates from 9.85-11.35Gbps with the internal synthesizer. With an external programmable divider, Centellax offers an expanded range of operation for lower data rate applications.

This option allows PRBS generation and error detection at rates around 5Gbps, 2.5Gbps and 1.25Gbps. This enables the BERT for use with different standards, and more capability for crosstalk applications.

This application note will cover the applications, the new block diagram of the TG1B1-A BERT, specifications of the new data rates, front panel operation, GPIB operation, and performance data.

Applications for lower operating rates

In addition to the 9.85-11.35Gbps standard operating rates, the new enhanced data rates include many standardized protocol rates. The standards covered by the new range of operation include:

- 1GbE (1.25Gbps)
- SONET OC-48 STM-16 (2.488Gbps)
- 2x GbE (2.5Gbps)
- PCI Express I (2.5Gbps)
- FB DIMM (2.5Gbps)
- PCI Express II (5.0Gbps)

Specifications for TG1B1-A

The range of each data rate is:

	Synth mode	Minimum step	Maximum Range	Minimum Range
External Clock	0	N/A	12.5Gbps	0.500Gbps
10G	1	10MHz	11.35Gbps	9.850Gbps
5G	2	5MHz	5.675Gbps	4.925Gbps
2.5G	4	2MHz	2.837Gbps	2.462Gbps
1.25G	8	1MHz	1.418Gbps	1.231Gbps

Table 1 – Data ranges and step sizes

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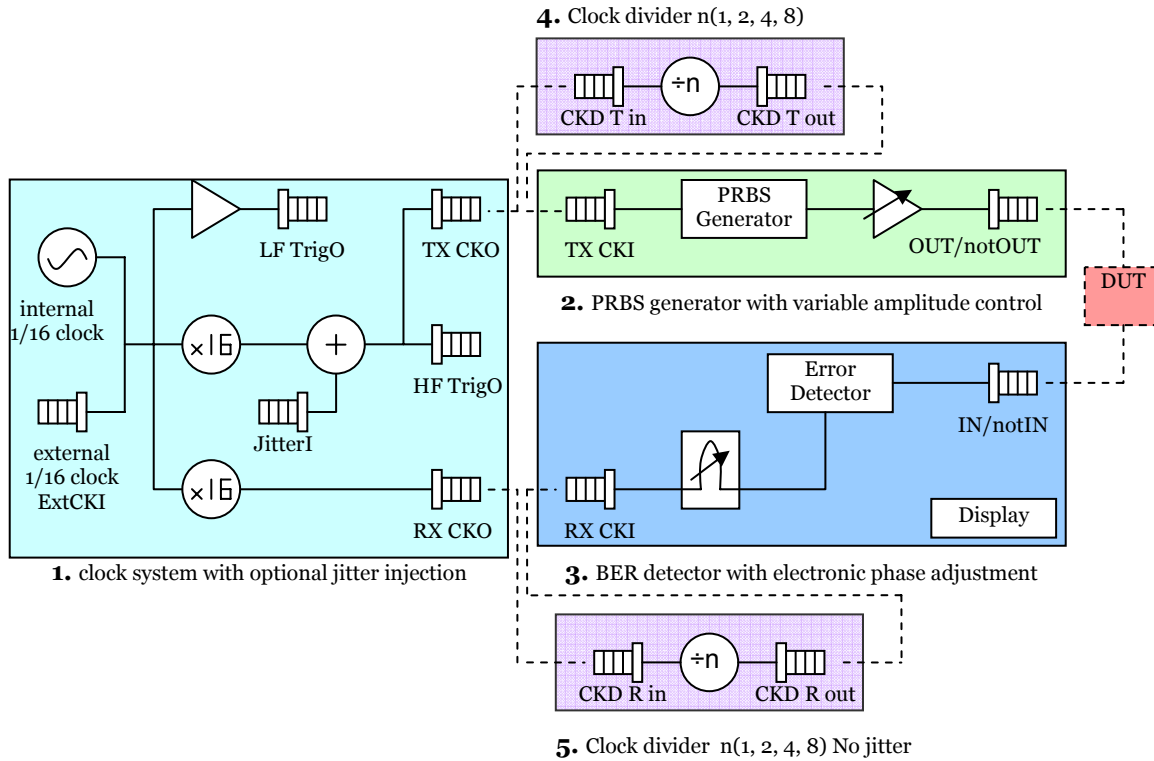


Figure 1 – 10G BERT system block diagram

In Figure 1, the block diagram of the TG1B1-A BERT is shown with the addition of blocks 4 & 5, which contain the external programmable clock dividers.

In block 4, the transmitter clock output (TX CKO) is connected to the divider input. The TX clock may optionally have jitter injected onto the source. In block 5, the receiver clock output (RX CKO) is connected to the divider input. This clock is separately divided, as it may not have the optional jitter injected onto the TX clock.

Both TX and RX clock dividers are controlled via the front panel interface, or the GPIB programming interface.

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Operation of Divider option

The programmable external dividers are controlled through the front panel with the **synth** configuration command. The values for **synth** are shown on Table 1. This option allows the internal clock to be disabled, and directs the divider to operate in the clock loops.

When supplying an external clock to RX CKI and TX CKI, with **synth** = 0, the frequency of operation must be programmed on the display. The display for frequency will show "X 10.000" meaning 10Gbps and the X denotes an external source.

The clock rate based on the divider amount for the internal synthesizer is shown in Table 1 where **synth** is set to 1, 2, 4, 8. The corresponding frequency ranges are shown in the Table 1.

The minimum step size for the frequency changes with the divide ratio changes if controlled with the front panel. Table 1 shows the step sizes which are used on the display with the front panel control. The GPIB allows for 1MHz step sizes regardless of the divider rate.

GPIB control of Divider Option

The GPIB control is also set using the **source** command. Using the **INTernal** step without any divider is the 10Gbps range.

```
:SOURCE:ROSC:SOURCE INTernal | EXTernal | DIV(N) N=2,4,8
:SOURCE:ROSC:FREQ
```

Examples:

```
:SOURCE:ROSC:SOURCE INT
:SOURCE:ROSC:FREQ 1125
```

```
:SOURCE:ROSC:SOURCE DIV2
:SOURCE:ROSC:FREQ 4990
```

```
:SOURCE:ROSC:SOURCE DIV4
:SOURCE:ROSC:FREQ 2500
```

```
:SOURCE:ROSC:SOURCE DIV8
:SOURCE:ROSC:FREQ 1250
```

The following example shows how to "incorrectly" program for an external divider

```
:SOURCE:ROSC:SOURCE INT
```

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:SOURCE:ROSC:FREQ 1250

Result: System errors=-222, "Data out of range"

It is very important to program the correct frequency which corresponds to the divider rate selected. The system error of -222 will result if this procedure is not followed. With the GPIB interface, the frequency step size is 1MHz, regardless of the divider rate.

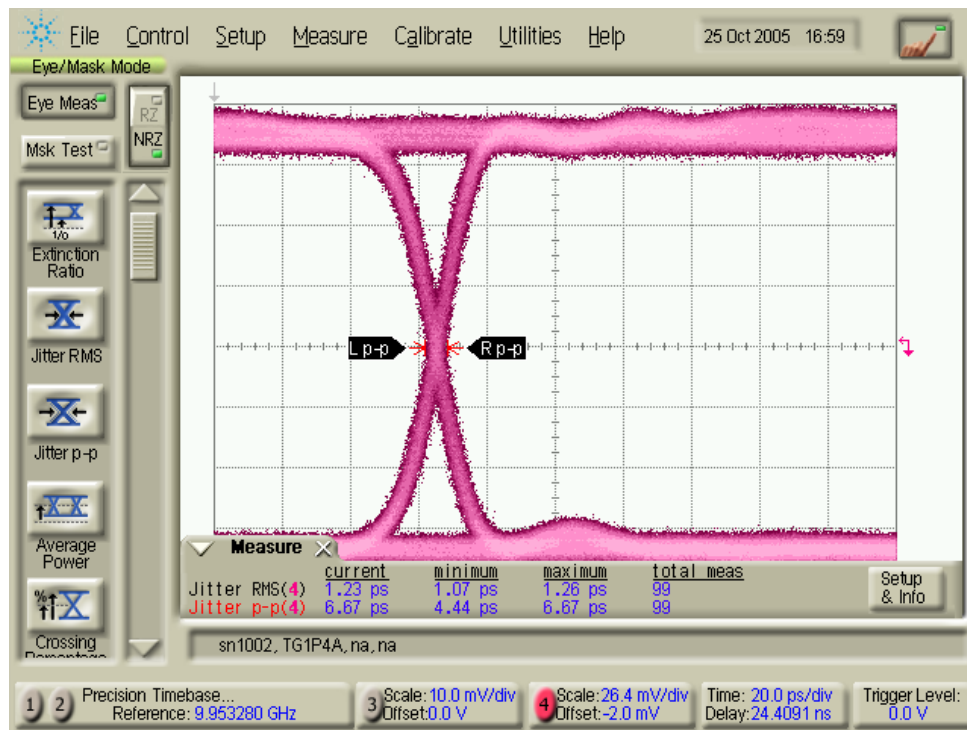


Figure 2 – 5Gbps waveform jitter measurements

Data rate	Rms jitter	Tj (pp jitter)
10.0Gbps	1.05ps	6.22ps
5.0Gbps	1.23ps	6.67ps
2.5Gbps	1.25ps	7.78ps
1.25Gbps	1.27ps	7.78ps

Table 2 – Performance of divided data rates

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Conclusions

The divider option for the TG1B1-A allows for multiple data rate testing over a large range without using an external synthesizer.

The jitter performance is maintained across all divider ratios for both random and deterministic jitter as shown in Table 2. The jitter measurement shown in Figure 2 was taken at 5.0Gbps, and illustrates the excellent performance.

The amplitude and phase controls still work without any changes. The jitter injection feature also works over all data ranges. The total amount of jitter injected on the waveform is reduced by the divider rate. This may require higher signals to be applied to the jitter input port for the same UI of jitter induced at the higher data rate.