

3.5-44 Gbps Clock and Data Demultiplexer

Operating Manual

PRELIMINARY



TR1D4A

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Additional information with regard to the applications and maintenance of this equipment may be available from time to time.

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Product Service

For information and pricing on standard factory service, please contact service@centellax.com.

Note: This product contains no user or factory adjustments. There is no calibration cycle or certificate.

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TR1D4A Operating Manual

Section 1: *Introduction*

This manual is to familiarize users with the fundamental operations of the Centellax TR1D4A Data Demultiplexer and Clock Divider.

Section 2: *Description*

The Centellax TR1D4A is an accessory which demultiplexes a high speed input bit stream into four low speed output bit streams. The input bit stream could be from 3.5Gbps to 44Gbps. The output bit streams would be from 0.875 to 11Gbps respectively.

The TR1D4A also has clock frequency dividers. The input clock frequency can be divided into certain ratios to get the four output clocks. The input clock is single ended. The four output clocks can be used as four single ended clocks or two pairs of differential clocks. The output clocks are AC coupled.

The table below gives the switch settings for different divide ratios.

Switches 1 and 2	or 3 and 4	or 5 and 6	or 7 and 8	Divide Ratio
0		0		1
1		0		1/8
0		1		1/4
1		1		1/2

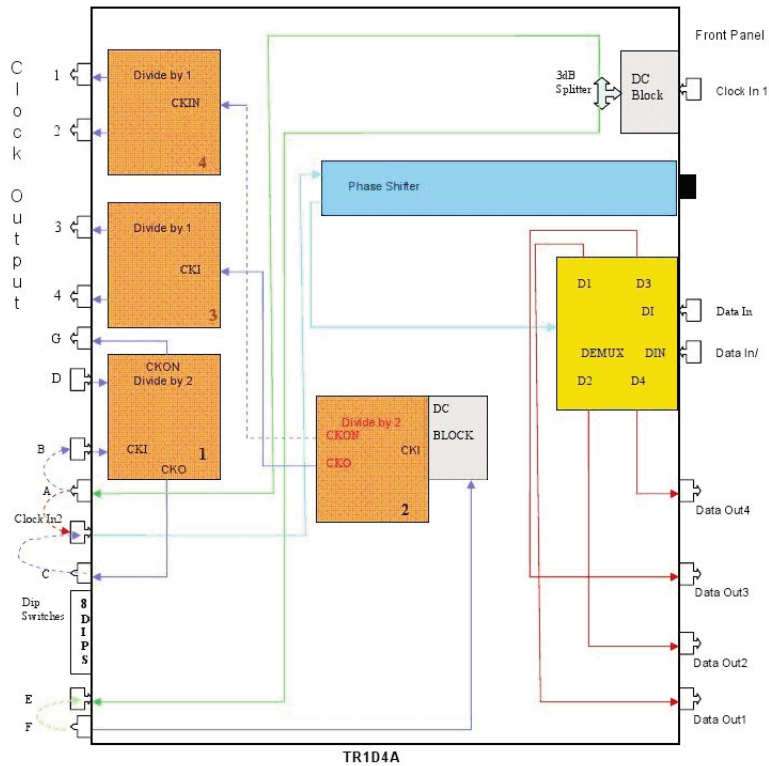
The divide ratio of the clock outputs 1 and 2 are the divide ratio of the divider 2 times the divide ratio of the divider 4. Similarly the divide ratio of the clock outputs 3 and 4 are the divide ratio of the divider 2 times the divide ratio of the divider 3. It is recommended to operate the dividers 1 and 2 at a ratio = 1/2 always. For any other ratios please contact the technical support for proper operations of the dividers.

B and D are the inputs and C and G are the outputs of the divider no.1. 3 and 4 are the outputs of the divider no. 3 and 1 and 2 are the outputs of the divider no. 4. The inputs and the outputs of the dividers are differential and the unused inputs and outputs should be terminated with 50Ω terminators. Connectors A through G at the rear panel are SMA female connectors.

The Data In and Data In/ are differential inputs for the data. These connectors are 1.85mm female connectors. If the data input is used single ended the input should be connected through a DC B block and the unused input should be terminated with a 50Ω 1.85mm terminator.

The Demux is a 1:4 Demux. The Demux operates using a half rate clock. The Demux samples the input data at the rising and the falling edges of its clock. The clock input to the Demux is routed through the phase shifter to align the clock edge to the data. By turning the phase shifter knob the clock edge can be aligned to the middle of the opening in the input data eye to get an error free output from the Demux. The phase shifter is a 60° per GHz, 18 turns phase shifter.

The demuxed data outputs are routed thru Data Out1 through Data Out4 connectors in the front panel. These are 2.92mm female connectors. They are single ended AC coupled outputs.



Section 3: Specification

Performance Specification Table

Description	Units	Min	Typ	Max
Input Bit Rate**	Gb/s	3.5	-	44
Output Bit Rate	Gb/s	0.875	-	11
Data Input Amplitude*,**	mVpp-se	150	600	1000
Data Output Amplitude	mVpp	210	240	270
Clock Input Amplitude	mVpp	470	600	1200
Clock Output Amplitude**	mVpp-se	-	500	-
Demux-by-4 Clock Input Frequency	GHz	1.75	-	22
Demux-by-2 Clock Input Frequency	GHz	3.5	-	22***

*Data input uses a V (f) connector. Data output and clock input use K (f) connectors. Clock output uses an SMA(f) connector.

**Differential input/output, can be used single-ended with proper 50ohm termination.

***Maximum input bit rate is 22Gb/s.

14G Operation:

1. Split the clock output of the clock source
2. One output of the splitter to the TG2P1A clock input
3. The other output to the TR1D4A Clock In1

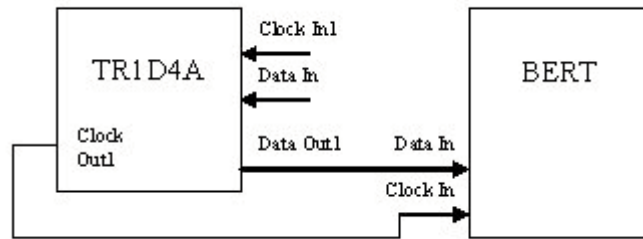
20G Operation:

1. TG1P2A Clk/1 to Clock In1
2. Loop A to B.
3. Loop C to Clock In2.
4. Loop E to F
5. UXD20PEs 1 and 2's ratios = $\frac{1}{2}$ and 3 and 4's ratio = 1.

40G Operation:

1. TG1P4A Clk/1 to Clock In1
2. Loop A to Clock In2
3. Loop E to F
4. UXD20PEs 3 and 4's ratios=1, 2's ratio = $\frac{1}{2}$ and 1's ratio is N/A

Section 4: Performance Verification



1. Connect the data output from a PRBS or a Programmable Pattern generator to the Data In or the Data In/ through a DC block. Make sure the polarity of the data output matches the polarity of the data input. Make sure the unused input is terminated. The inputs can be connected differentially taking care of the polarity
2. Connect the clock input to the generator
3. Connect the input clock of the TR1D4A to the Clock In1. This input is internally DC blocked.
4. Connect one of the TR1D4A clock outputs to the error detector clock input. Make sure the divide ratio is such that the rate of the divided clock is one fourth the data rate.
5. Connect one of the TR1D4A data outputs to the error detector data input.
6. Turn on and setup the error detector
7. Turn on the TR1D4A and the generator
8. Adjust the phase shifter of the TR1D4A until you read zero ber in the error detector.
9. Repeat the steps for the other data outputs and clock outputs of the TR1D4A.

The block diagram of the TR1D4A is as given on the following page. The Demux needs a half rate clock to function. The clock is fed through the Clock In1 connector in the front panel. The Clock In1 is DC blocked. The divider no.1 is used to divide the input clock rate by 2 to feed a half rate clock to the Demux. This is done by connecting A to B and C to Clock In2 at the rear panel. This is necessary to use our TG2P1A and TG1P2A PRBS Generators because they are operated by full rate clocks.

The divider no.1 is not necessary if the input clock through Clock In1 is a half rate clock. In this case A is connected to Clock In2 directly without going through the divider no.1. This is required to use our TG1P4A PRBS Generator because it is operated by a half rate clock.

E is connected to F at the rear panel to divide the rate of the input clock through Clock In1 further down to get the four divided clock outputs at the rear panel. These divided clocks can be used with the BERTS for error detection and/or can be used with the DCA. The dip switches at the rear panel would enable setting the divide ratios of the dividers. There are 2 switches for each divider making a total of 8 switches. The numbers on the top of the switches correspond to the numbers of the dividers. The numbers of the dividers are marked in the block diagram and their relative locations are as shown.