

## 40 Gb/s 4:1 Multiplexer Module



### Features

- Half rate clock
- High Input Sensitivity
- Wide Operating Range, 2-44 Gb/s
- Low Output Jitter
- Low Power Consumption
- Fast Output Rise/Fall Times

### Description

The MS4S1V1M is a broadband 4 to 1 MUX with continuous coverage from 2 to 44 Gb/s. The four quarter-rate data inputs are single-ended and AC-coupled, while the full-rate data output is fully differential and DC-coupled. The MUX accepts a half-rate input clock and returns a quarter-rate output clock for driving other circuits. A clock crossing adjustment pin allows correction for duty cycle distortion. Power supply bias of negative 3.6V is required.

### Applications

The MS4S1V1M can be used with existing equipment to generate higher rate bit streams for use in telecom applications up to 44 Gb/s. Broadband test systems will benefit from the low power dissipation, precision connectors, and excellent output waveform characteristics. The compact size of the module allows the MS4S1V1M to be placed at the measurement plane, reducing or eliminating artifacts related to long cables.

### Operating Conditions

| Parameter | Minimum | Typical | Maximum | Units |
|-----------|---------|---------|---------|-------|
| Vee       | -3.7    | -3.6    | -3.5    | V     |

### Key Specifications @ 25°C

Vee = -3.6V, Iee = 560mA, Zo = 50 Ω

| Parameter                | Minimum | Typical | Maximum | Units |
|--------------------------|---------|---------|---------|-------|
| <b>Data Input</b>        |         |         |         |       |
| Bit Rate                 | 0.5     | -       | 11      | Gb/s  |
| Amplitude                | 100     | -       | 1000    | mVpp  |
| <b>Clock Input</b>       |         |         |         |       |
| Frequency                | 1       | -       | 22      | GHz   |
| Amplitude                | 200     | -       | 1400    | mVpp  |
| Power                    | -10     | -       | +7      | dBm   |
| <b>Data Output</b>       |         |         |         |       |
| Bit Rate                 | 2       | -       | 44      | Gb/s  |
| Amplitude (Single-Ended) | 450     | 500     | 600     | mVpp  |
| Jitter RMS               | -       | 0.5     | 1       | psec  |
| Jitter Pk-Pk             | -       | 2.5     | 4       | psec  |
| Rise Time (20/80)        | -       | 8       | 10      | psec  |
| Fall Time (20/80)        | -       | 8       | 10      | psec  |
| SNR                      | 10      | -       | -       | dB    |
| <b>Clock Output</b>      |         |         |         |       |
| Frequency                | 0.5     | -       | 10      | GHz   |
| Amplitude                | 300     | -       | 450     | mVpp  |

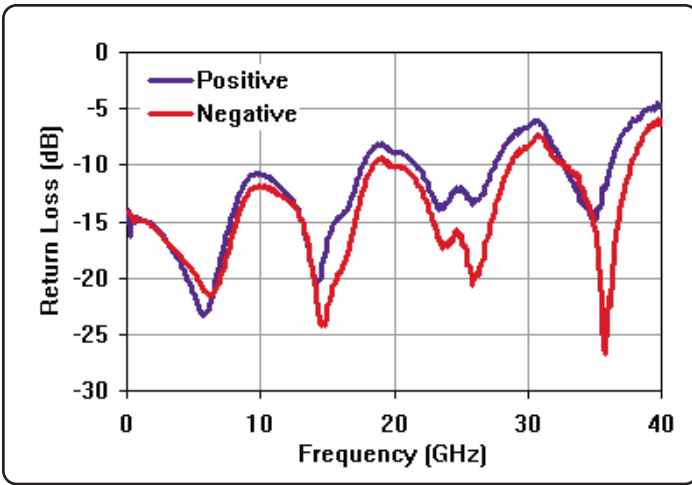


Figure 1: Data Output Return Loss

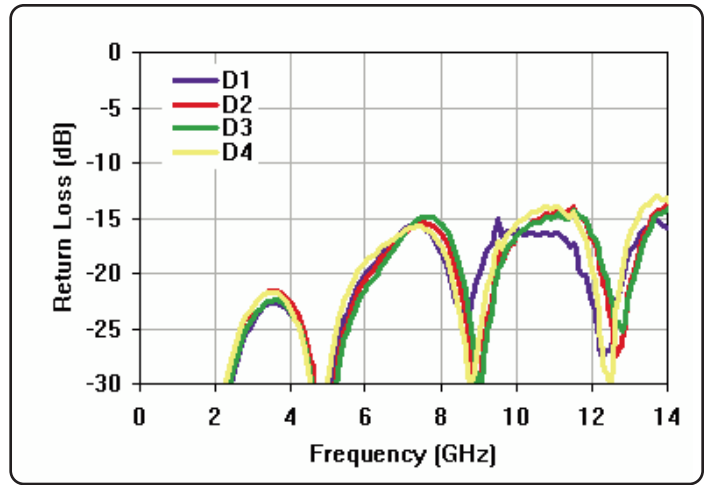


Figure 2: Data Input Return loss

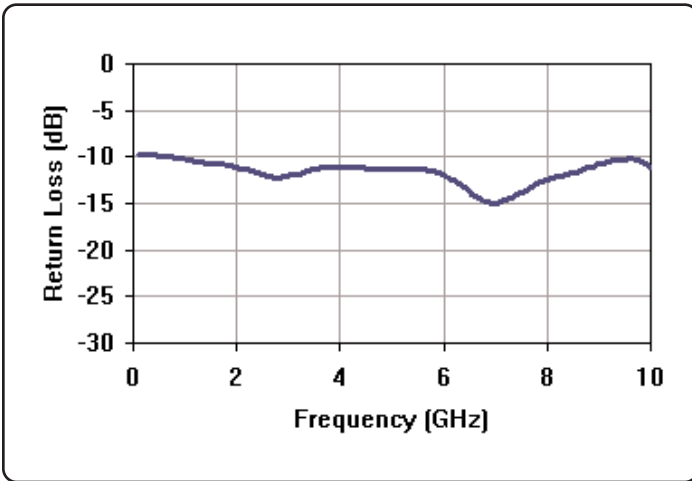


Figure 3: Clock Output Return Loss

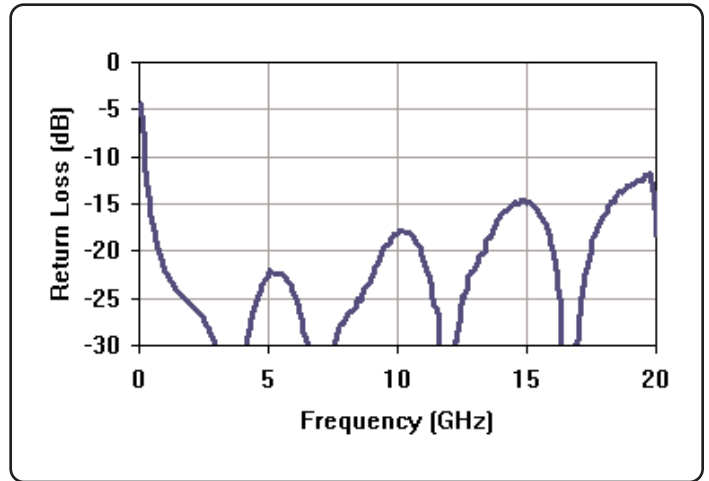


Figure 4: Clock Input Return Loss

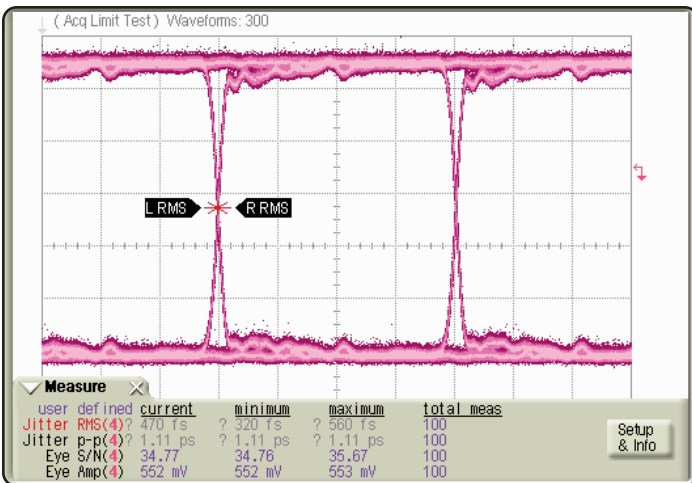


Figure 5: Data Output Waveform @ 5Gb/s  
Four 1.25Gb/s, 2e31-1 Data Inputs

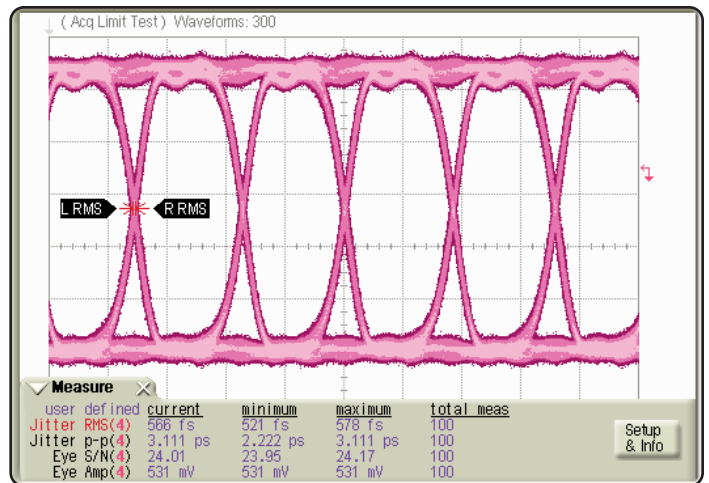


Figure 6: Data Output Waveform @ 28Gb/s  
Four 7Gb/s, 2e31-1 Data Inputs

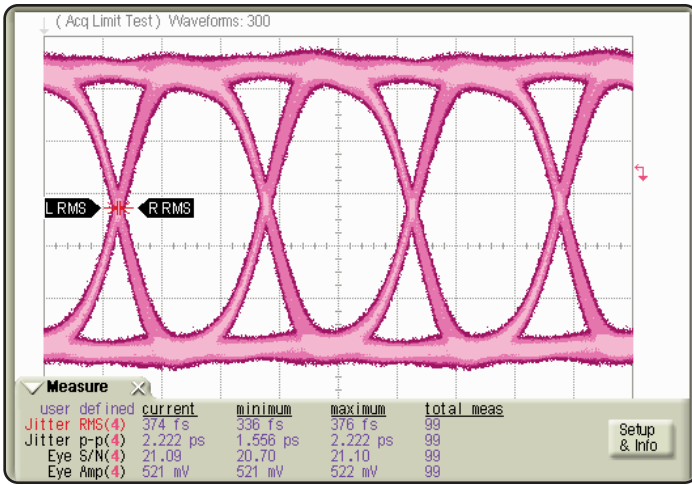


Figure 7: Data Output Waveform @ 40Gb/s  
Four 10Gb/s, 2e31-1 Data Inputs

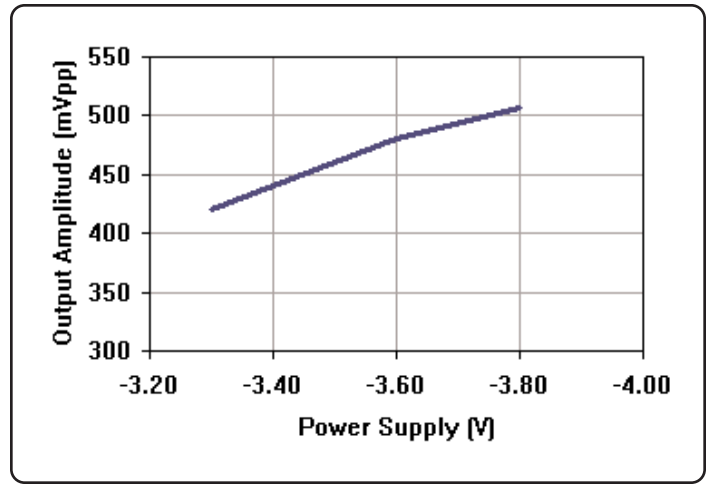


Figure 8: Data Output Amplitude vs Power Supply  
Data Rate @ 40Gb/s

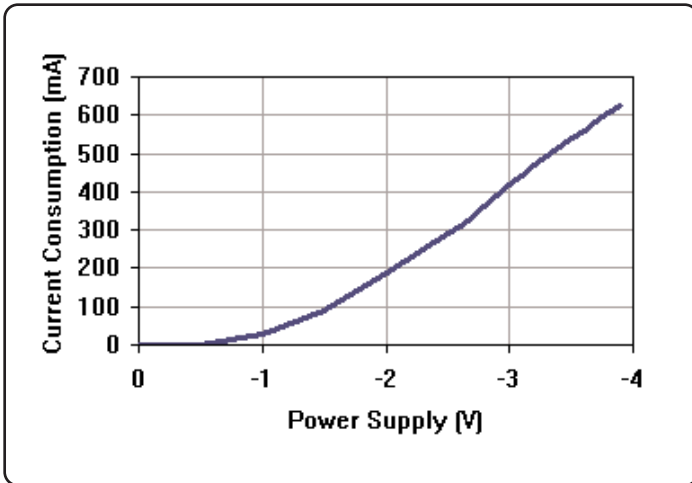


Figure 9: Power Supply Current vs Voltage

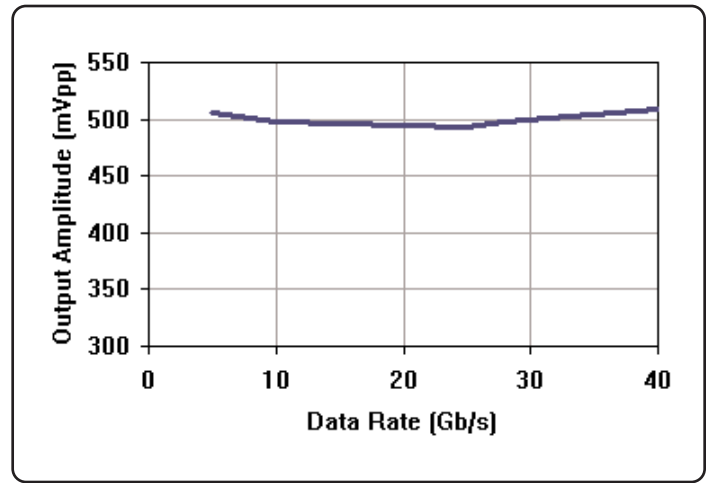


Figure 10: Data Output Amplitude vs Data Rate  
Power Supply @ -3.6V

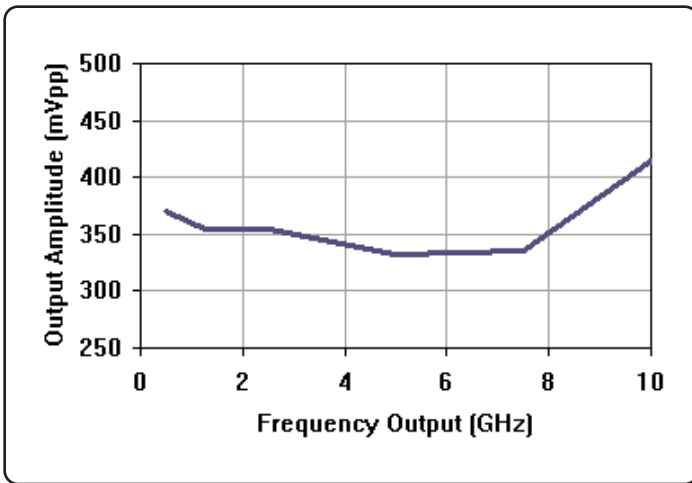


Figure 11: Clock Output Amplitude vs Frequency  
Power Supply @ -3.6V

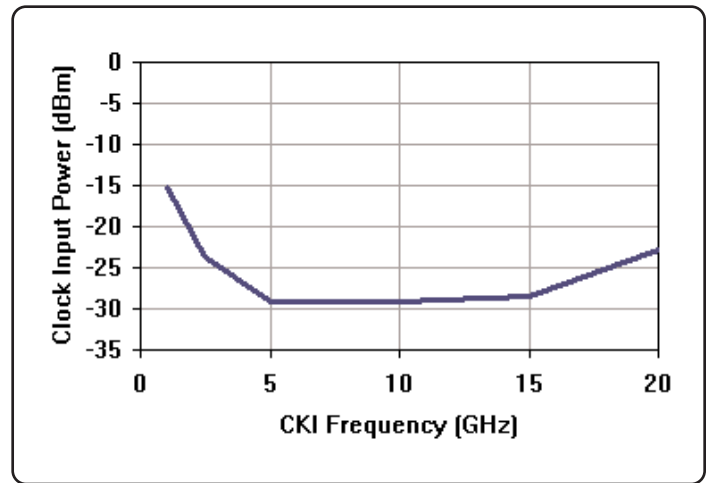
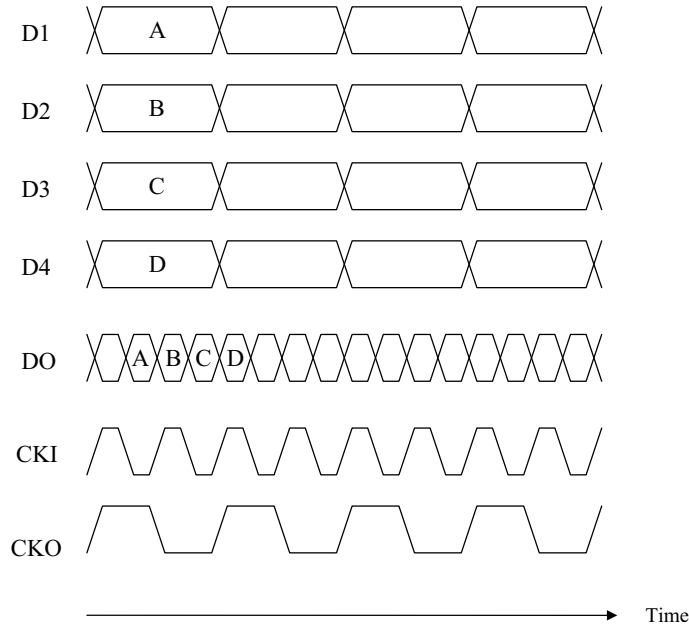


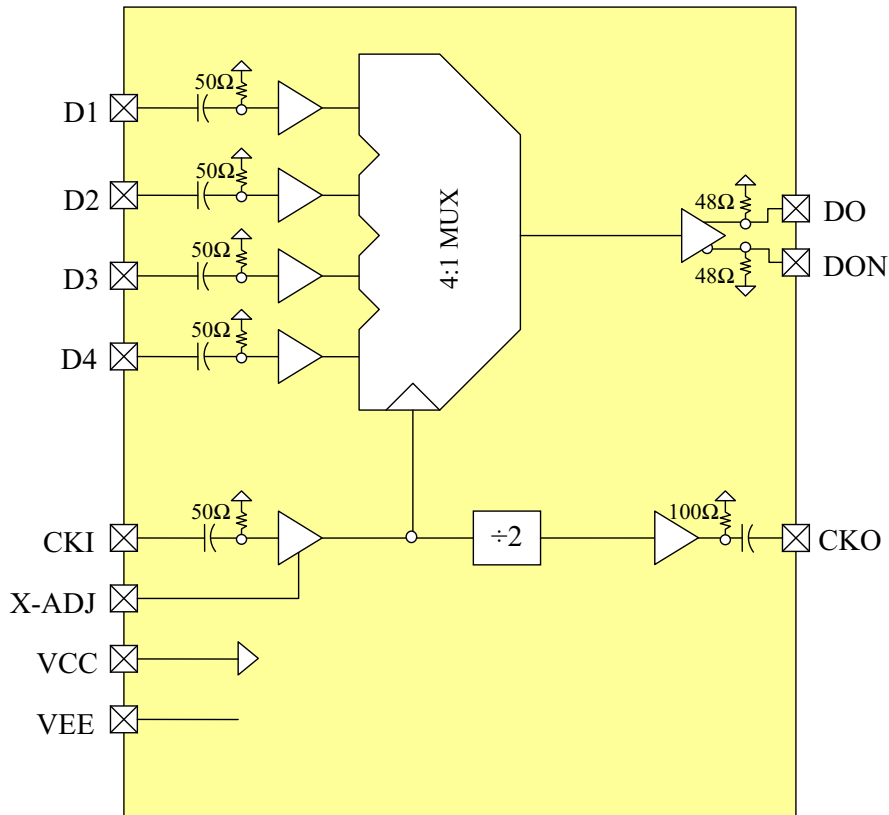
Figure 12: Clock Input Sensitivity vs Frequency  
Power Supply @ -3.6V

## Timing Diagram



Note: Phase relationship between signals not implied.

## Functional Block Diagram

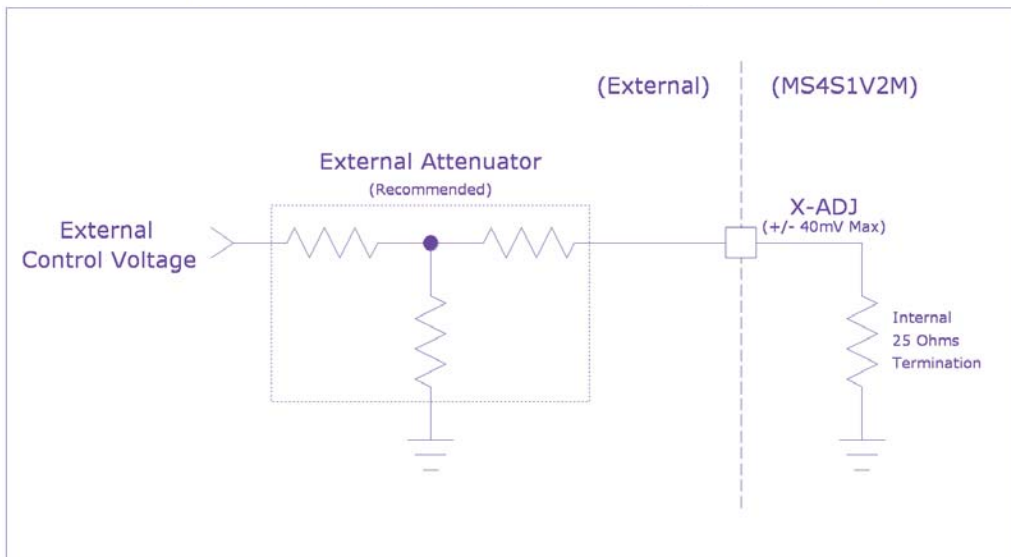


## Clock Cross-Over Adjustment

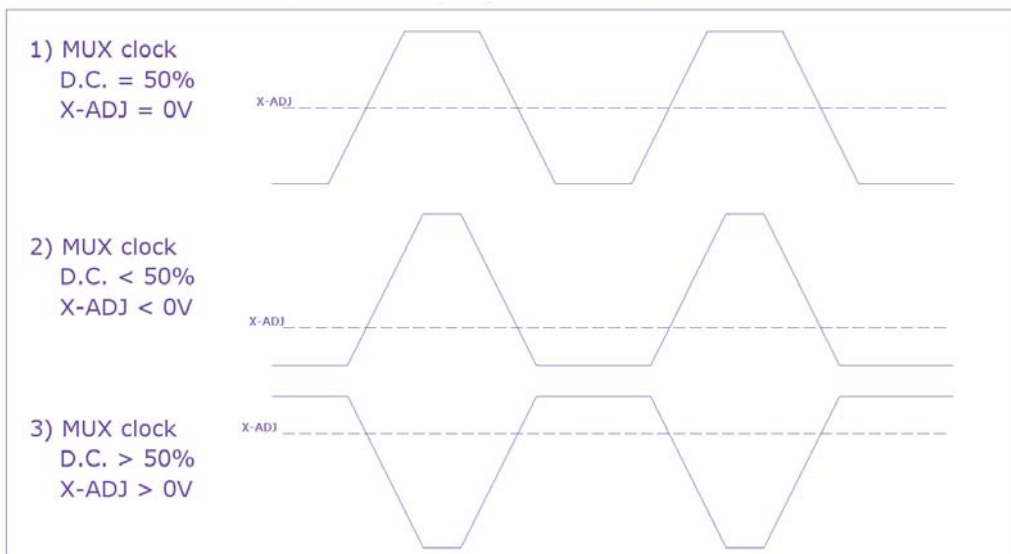
The duty cycle of the input clock can have adverse effects on eye quality when deviating from 50%. Non-50% duty cycle is referred to as “duty cycle distortion” (DCD). DCD on the input clock will directly translate to double-tracking on the output eye, because adjacent bits would have unequal pulse-widths. DCD can happen by various means. For example, amplifiers operating in the non-linear regime when driven with large signals can often lead to un-evenly clipped waveforms and hence DCD. As another example, mismatches in differential circuits can cause voltage offsets between the differential signals thus leading to DCD. For these reasons, DCD can vary with frequency, temperature, and process variations.

The MS4S1V1M addresses the issue of clock DCD by providing an analog cross-over control for the input clock. This control pin allows the user to correct for a wide range of clock DCD. The cross over control is terminated internally with a 25 Ω load, and can accommodate a voltage range of +/-40mV. An external attenuator or resistor in series is recommended to prevent from overdriving and damaging this sensitive input (see figure for example). Note that the cross-over range is limited to the rise/fall times of the input clock.

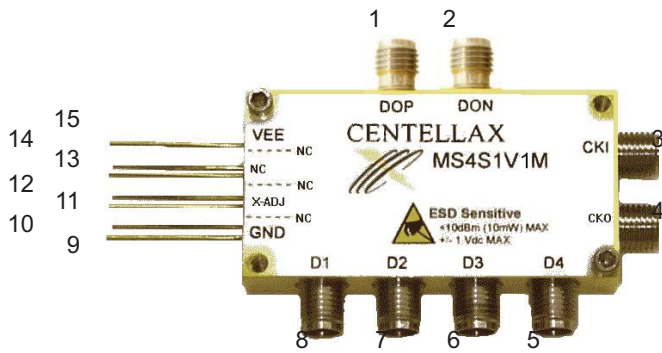
### MS4S1V1M Clock Cross-Over Adjust Control



### Clock Duty Cycle Waveforms



## Module Outline



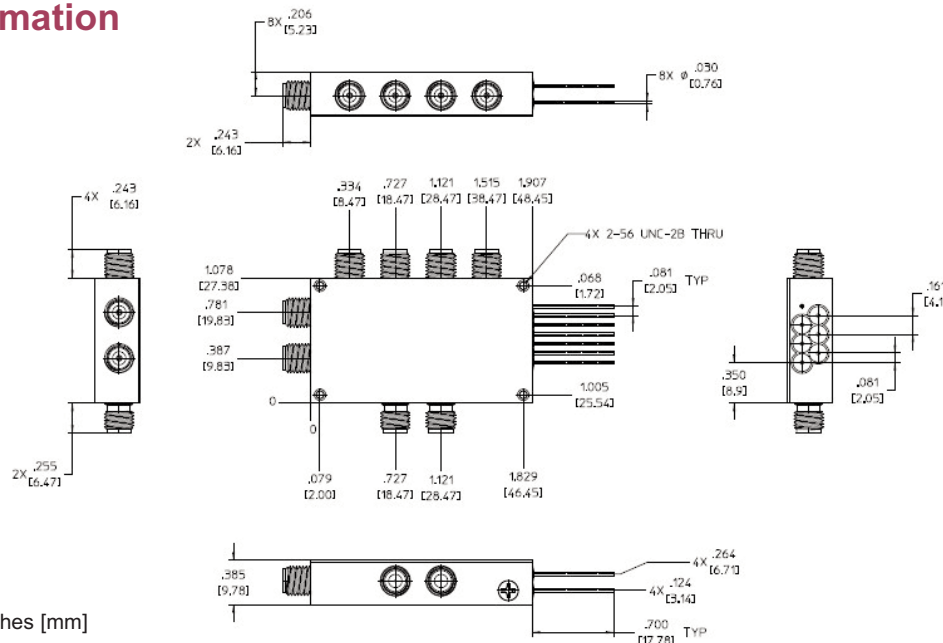
## Absolute Maximum Ratings

| Parameter                        | Value      | Unit |
|----------------------------------|------------|------|
| Supply Voltage (VEE)             | -4.0       | V    |
| Clock Input Power (CKI)          | +10        | dBm  |
| Data Input (D1, D2, D3, D4)      | 2.0        | Vpp  |
| DC voltage (CKI, D1, D2, D3, D4) | ±0.5       | V    |
| Operating Temperature            | 0 to 70    | °C   |
| Storage Temperature              | -85 to 125 | °C   |

## Pin Description

| Name  | PIN       | DESCRIPTION                         | NOTES   | CONNECTOR   |
|-------|-----------|-------------------------------------|---|-------------|
| DOP   | 1         | Data Channel Output                 | Positive Terminal of Differential Output                        | 2.92 mm (K) |
| DON   | 2         | Data Channel Output                 | Negative Terminal of Differential Output                        | 2.92 mm (K) |
| CKI   | 3         | Clock Input                         | 1/2 of Bit Rate, e.g. 22GHz for 44Gb/s<br>Single-ended input    | 2.92 mm (K) |
| CKO   | 4         | Clock Divided Output                | 1/4 of Bit Rate, e.g. 11 GHz for 44Gb/s,<br>Single-ended output | 2.92 mm (K) |
| D4    | 5         | Data Channel Input - Bit Position 4 | Trailing/last serial data bit                                   | 2.92 mm (K) |
| D3    | 6         | Data Channel Input - Bit Position 3 | -   | 2.92 mm (K) |
| D2    | 7         | Data Channel Input - Bit Position 2 | -   | 2.92 mm (K) |
| D1    | 8         | Data Channel Input - Bit Position 1 | Leading/first serial data bit                                   | 2.92 mm (K) |
| VCC   | 9         | RF & DC Ground                      | Chassis/Module Connection                                       | -           |
| X-ADJ | 11        | Clock Cross-Over Adjust             | +/- 40mV max, 25Ω   | -           |
| VEE   | 15        | Negative Supply Voltage             | -3.6V @560mA, DC PIN  | -           |
| NC    | 10, 12-14 | No Connect                          | -   | -           |

## Packaging Information



Note: all measurements in inches [mm]