

5 - 18GHz Surface Mount Amplifier with Integrated Bias



Features

- Wide operating range: 5-18GHz
- 3.3V, 100mA drain bias (gate N/C) for gain and NF:
 - 13 ±0.4dB gain, 7dB NF, 16dBm Psat, 13.5dBm P-1
- 5V, 130mA drain bias (gate N/C) for power:
 - 12.5 ±0.7dB gain, 9dB NF, 19.5dBm Psat, 17dBm P-1
- Single supply voltage with self-biasing gate
OR direct control of both gate and drain stages

Applications

The UA5M15MP is ideally suited for:

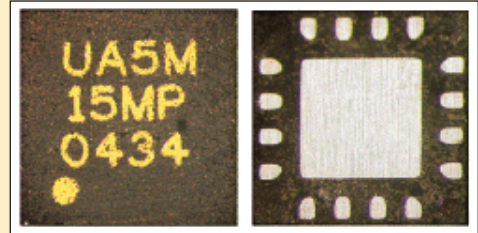
- Point-to-point and point-to-multipoint digital radio
- Spread spectrum broadband communications
- LO driver or mixer isolation amplifier
- General isolation and gain block amplifier

Description

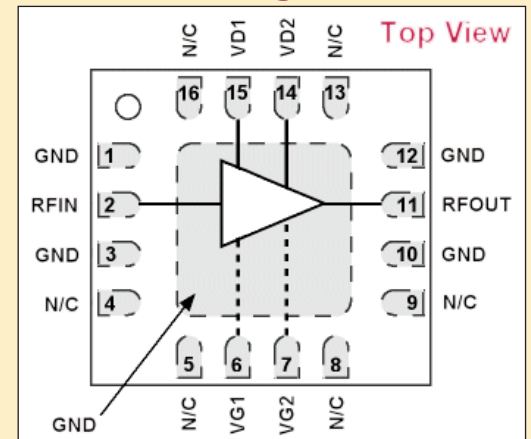
The UA5M15MP is a two-stage pHEMT amplifier MMIC in a Pb-free leadless plastic QFN package. The IC features a positive gain slope that offsets package loss, resulting in a SMT part with excellent gain flatness across a broad bandwidth. The device can be operated at 5V 130mA for power applications, or 3.3V 100mA for low-noise and gain.

Surface Mount Package

- 16-pin **Pb-free** SMT QFN package
- 3x3mm pkg size; 0.5mm pad pitch



Functional Diagram



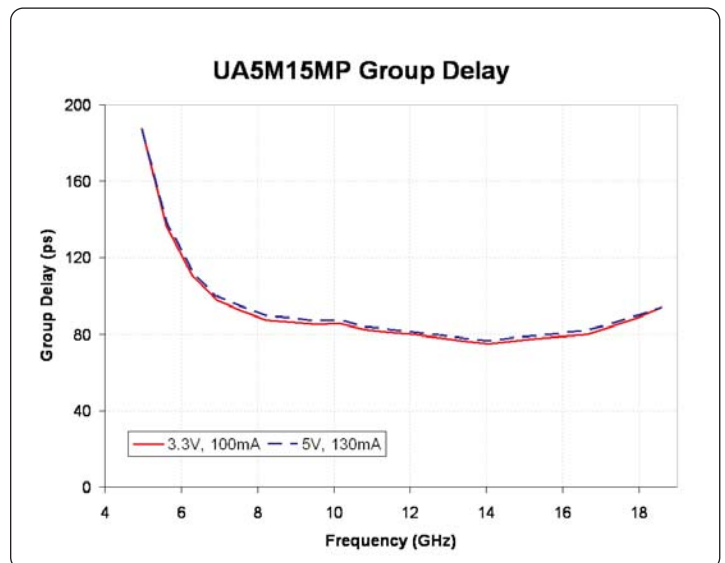
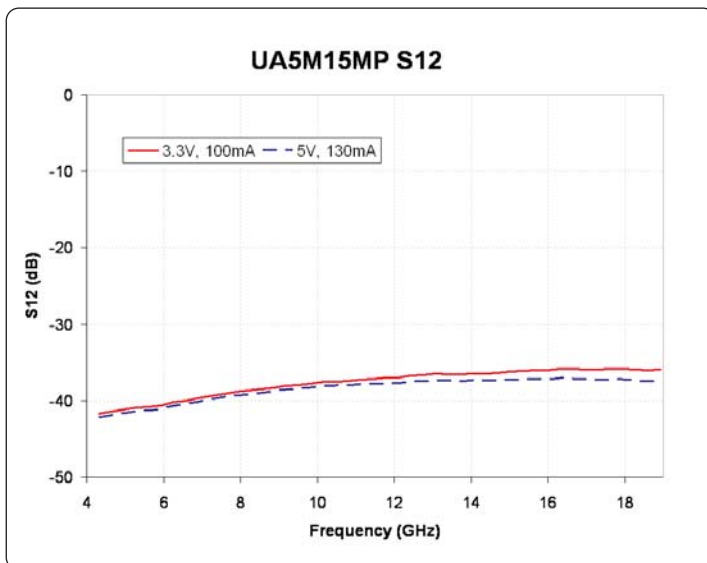
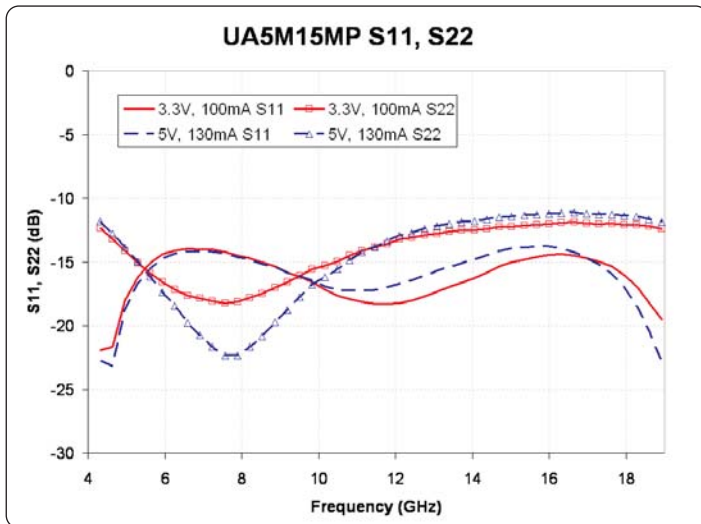
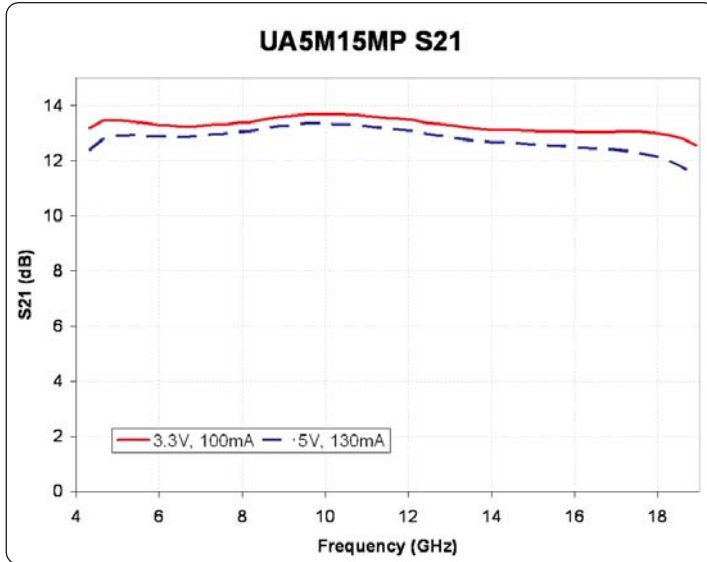
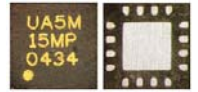
Key Specifications

$V_d=V_{d1}=V_{d2}$, $V_g=V_{g1}=V_{g2}$, $I_d=I_{d1}+I_{d2}$, $Z_o=50\Omega$

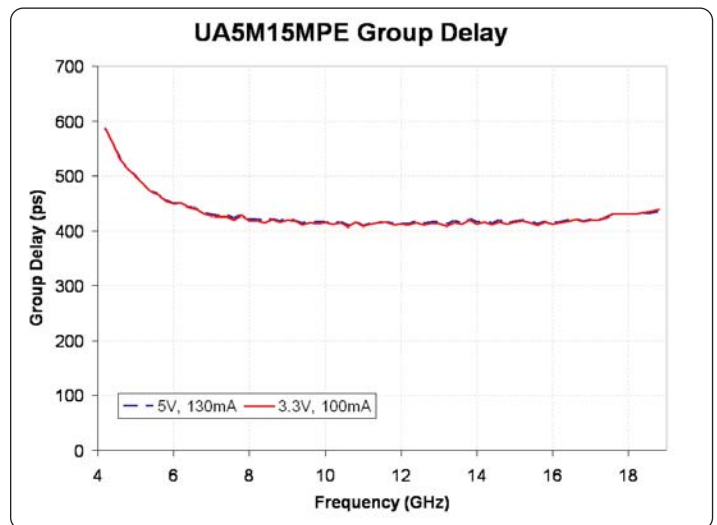
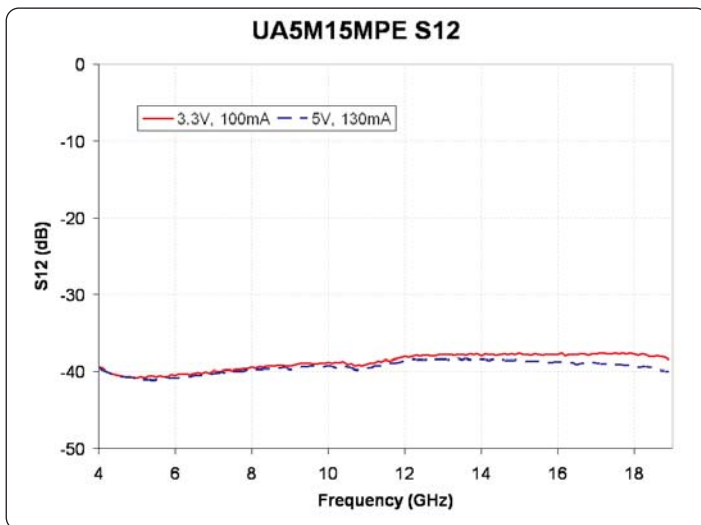
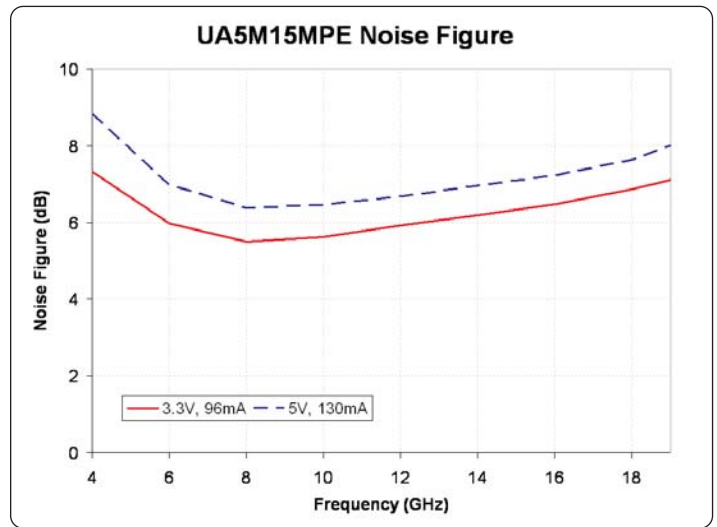
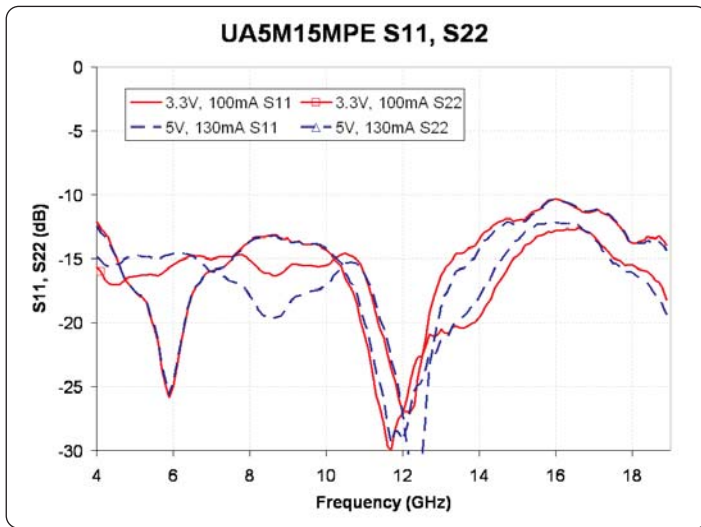
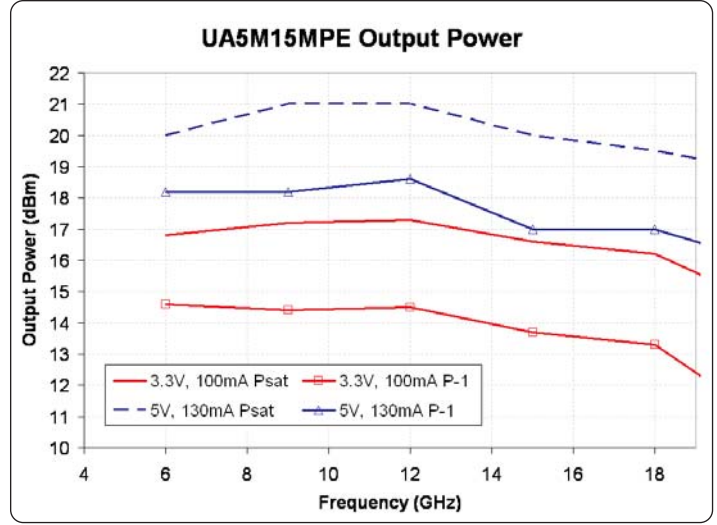
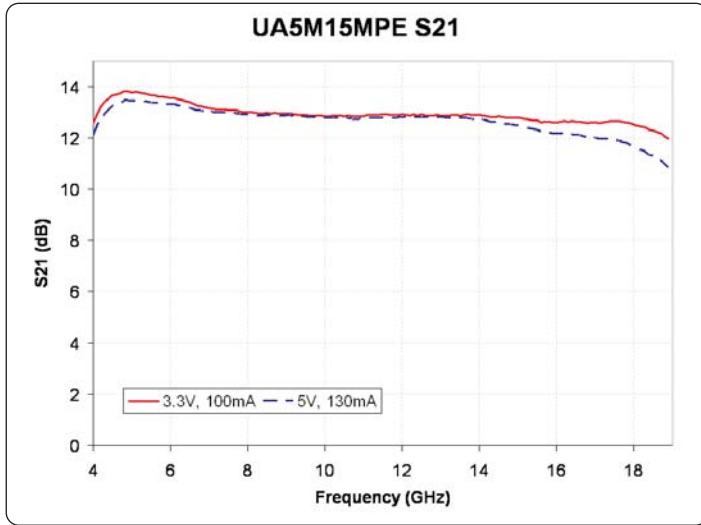
Specifications pertain to measurements with RF probes and DC bias cards @ 25°C

Frequency Range: 5 - 18GHz		Gain Bias: $V_d=3.3V$, $V_g=N/C$, $I_d=100mA$			Power Bias: $V_d=5V$ $V_g=N/C$, $I_d=130mA$		
Parameter	Description	Min	Typ	Max	Min	Typ	Max
S21 (dB)	Small Signal Gain		13			12.5	
Flatness (±dB)	Gain Flatness		0.4			0.7	
S11 (dB)	Input Match		-14			-14	
S22 (dB)	Output Match		-11			-11	
S12 (dB)	Reverse Isolation		-35			-35	
P_{-1dB} (dBm)	1dB Compressed Output Power		13.5			17	
P_{sat} (dBm)	Saturated Output Power		16			19.5	
NF (dB)	Noise Figure		7			9	

Typical probed QFN package (UA5M15MP)



Typical connectorized evaluation board (UA5M15MPE)



Supplemental Specifications

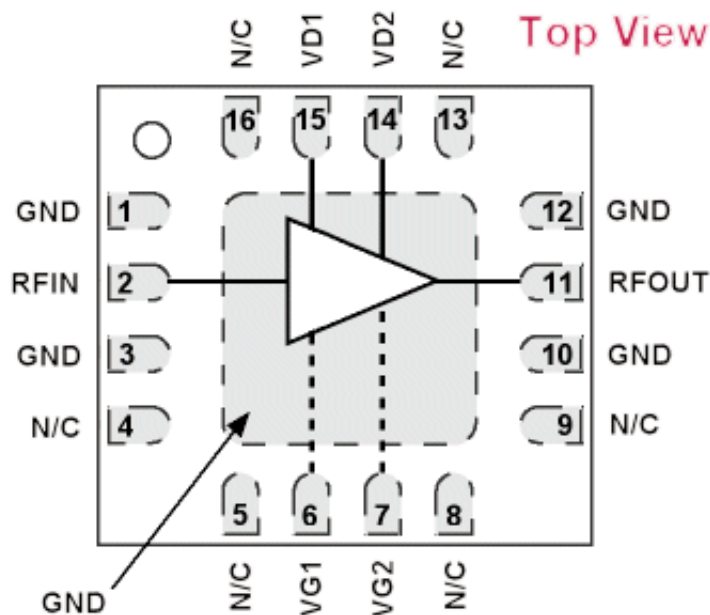
Parameter	Description	Min	Typ	Max
Vd1	Drain Bias Voltage FET1		3.3V, 5V	6V
Id1	Drain Bias Current FET1			90mA
Vd2	Drain Bias Voltage FET2		3.3V, 5V	6V
Id2	Drain Bias Current FET2			110mA
Vgg1	Gate Bias Voltage FET1	-4V	N/C	+1V
Vgg2	Gate Bias Voltage FET2	-4V	N/C	+1V
P_{in}	Input Power (CW)			12dBm
P_{dc}	Power Dissipation		0.33W, 0.65W	
T_{ch}	Channel Temperature			150°C
Θ_{ch}	Thermal Resistance ($T_{case}=85^{\circ}C$)		60°C/W	

Typical Bias Values

Vdd (V)	Idd (mA)	App
+5.0	130	power
+4.0	110	
+3.3	100	gain
+2.5	79	low-noise

Amplifier will operate over the full voltage range shown above

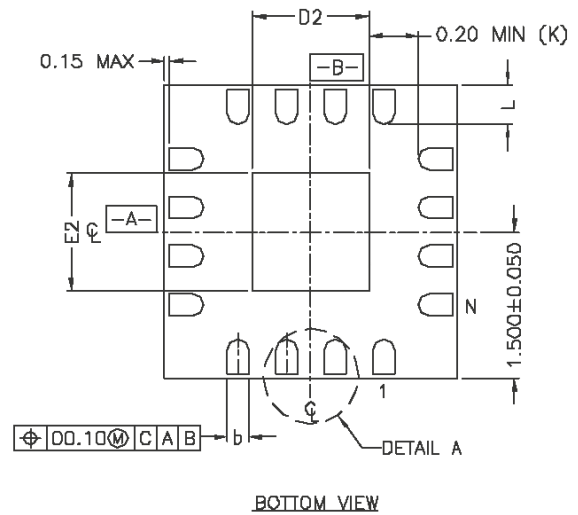
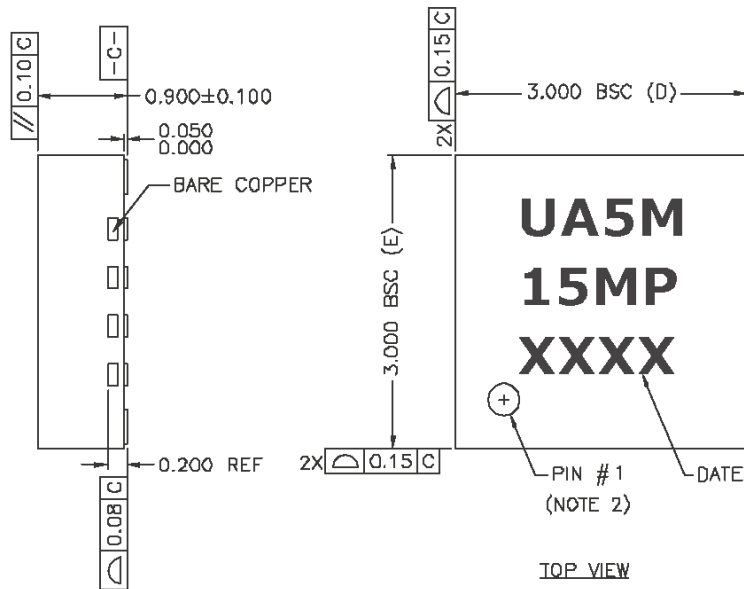
Functional Block Diagram



Pin Descriptions

Number	Function	Description
4, 5, 8, 9, 13, 16	N / C	No connection necessary, may be connected to DC / RF ground
1, 3, 10, 12 + paddle	GND	Must be connected to DC / RF ground
2, 11	RF IN, OUT	AC coupled and matched to 50Ω
6, 7	VG1, VG2	Optional 1st and 2nd gate bias lines, requires >100pF low-freq bypass capacitor if used
14, 15	VD1, VD2	1st and 2nd drain bias lines, requires >100pF low-freq bypass capacitor and clean power supply

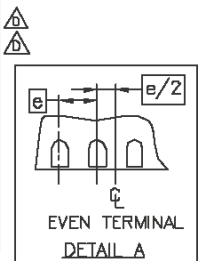
Physical Characteristics



Package Notes

1. Conforms to JEDEC MO-220, revision 1
2. Pin 1 ID indicated by dot on top of package
3. All units millimeters, not to scale
4. Pkg is 100% Pb free (lead free)
5. Leadframe base is 0.2mm Cu 194 FH with Ag-ring finish
6. Solder plate is 100% Sn
7. All ground leads and center paddle must be connected to RF ground

SYMBOL	VARIATION		
	MIN	NOM	MAX
e	0.50 BSC		
b	0.18	0.23	0.30
E2	1.80	1.70	1.80
D2	1.80	1.70	1.80
L	0.35	0.40	0.45
N	16 LD		
ND	4		
NE	4		
JEDEC VARIATION	N/A		
INTERNAL FEATURE	N/A		
PKG CODE	VQ 016		



Lead free (Pb-free)

The UA5M15MP QFN package contains no lead (Pb) and eliminates the need for costly re-qualification efforts, which are necessary to conform to the European mandated "Restricted use of Hazardous Substances" (RoHS) compliance.

Applications Support

Additional application support is available upon request. Visit the Centellax website for more information: <http://www.centellax.com/products/microwave/smt/UA5M15MP.shtml>.

Thermal Heat Sinking:

To avoid damage and for optimum performance, you must observe the maximum channel temperature and ensure adequate heat sinking. PCB ground planes are not sufficient, the backside of the QFN must be soldered to the PCB, and PCB filled or plated vias must be used to conduct heat away from this contact.

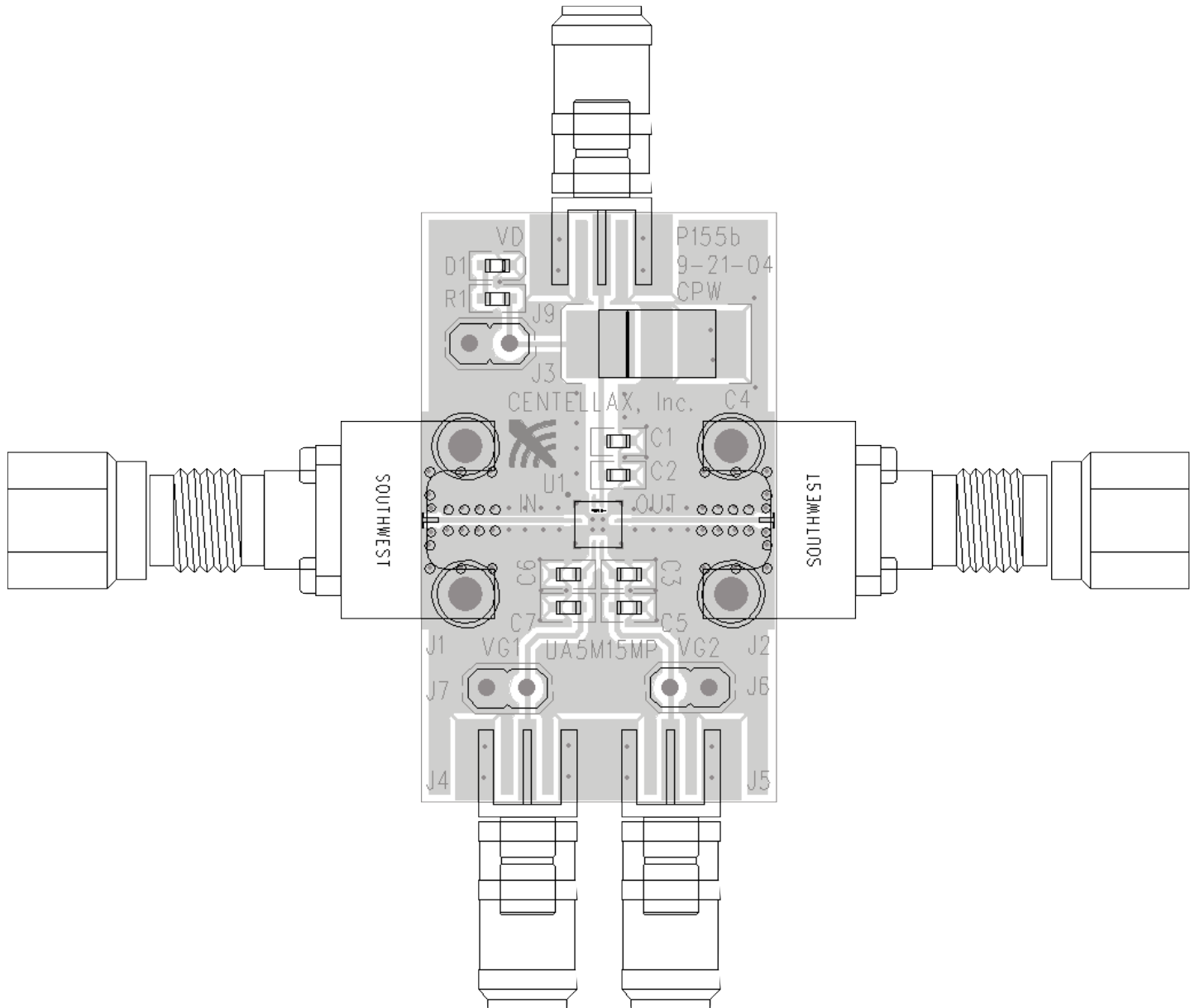
ESD Handling and Bonding:

This package is ESD sensitive; preventive measures should be taken during handling and solder attach.

Solder paste and flux screen printing is recommended.

UA5M15MPE Evaluation Board

Evaluation Board Layout

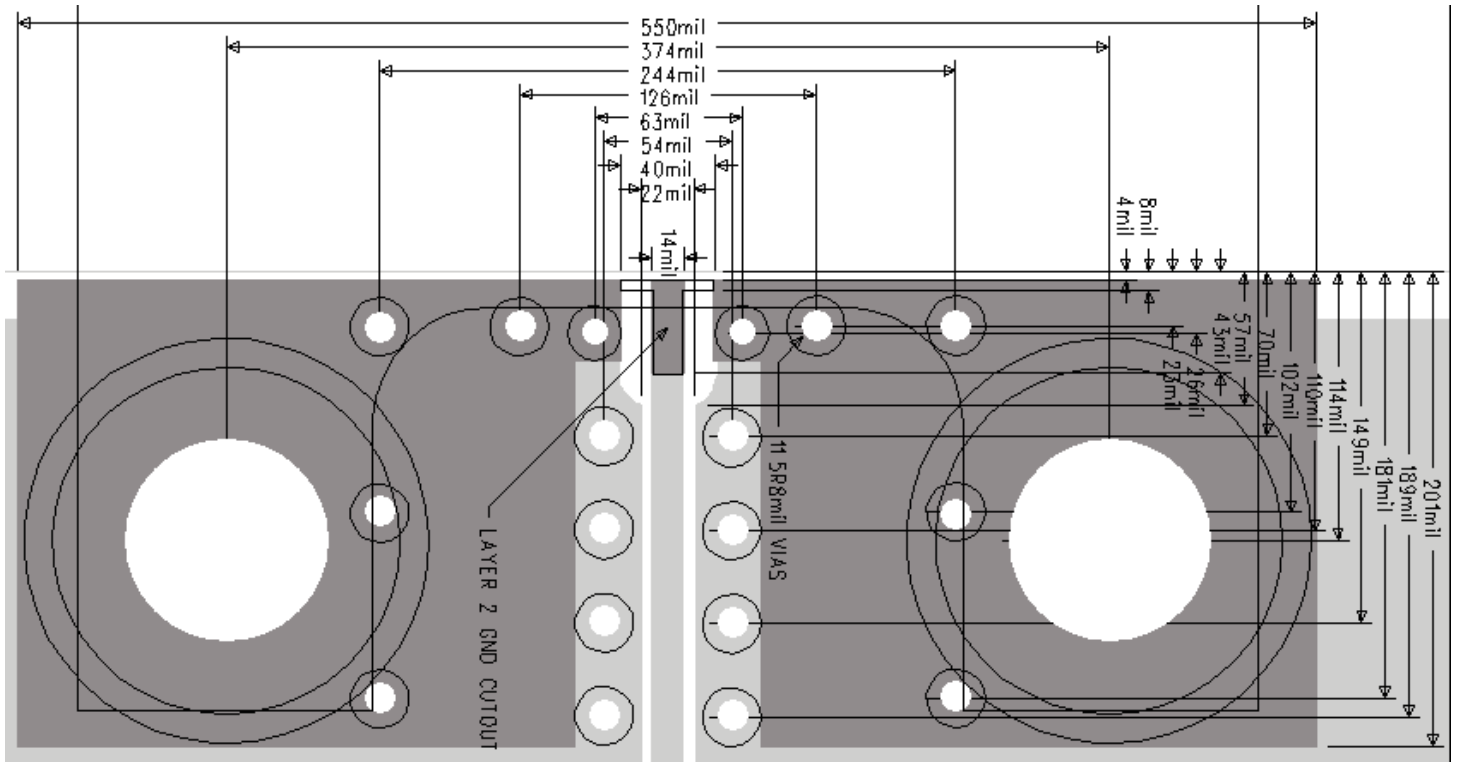


Component List

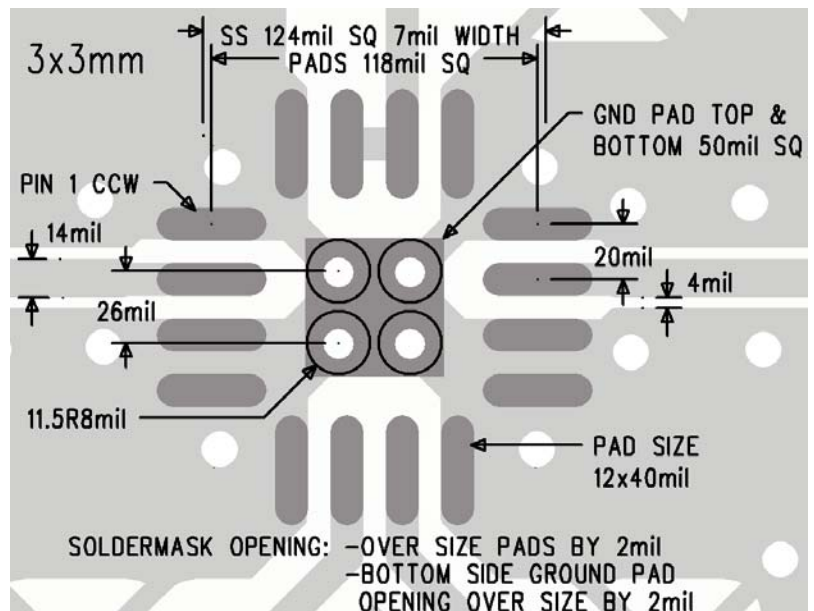
C1, C5, C7	DigiKey 399-1281-1-ND	C2, C3, C6	DigiKey 445-1283-1-ND
C4	DigiKey 399-1620-1-ND	D1	DigiKey P521CT-ND
J1, J2	SouthWest 1092-04A-5	J3, J6, J7	DigiKey S2011-36-ND
J4, J5, J9	Allied Elec. 903-518J-51P	R1	DigiKey P1.00KHCT-ND
U1	Centellax UA5M15MP		

UA5M15MPE Evaluation Board

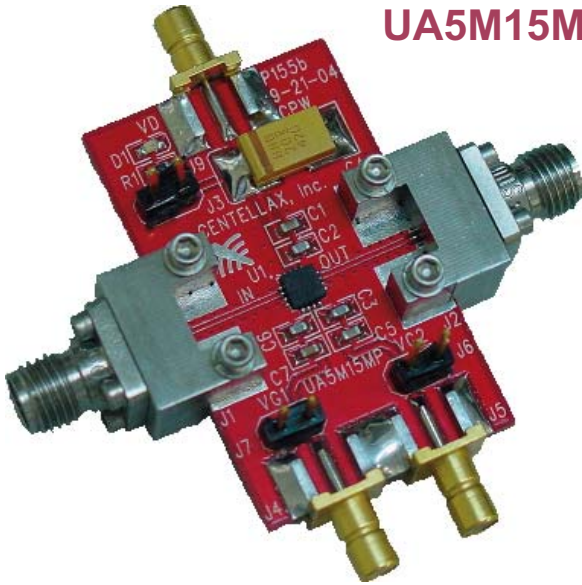
Evaluation Board Layout - Connector Attach Details



Evaluation Board Layout - QFN Land Details

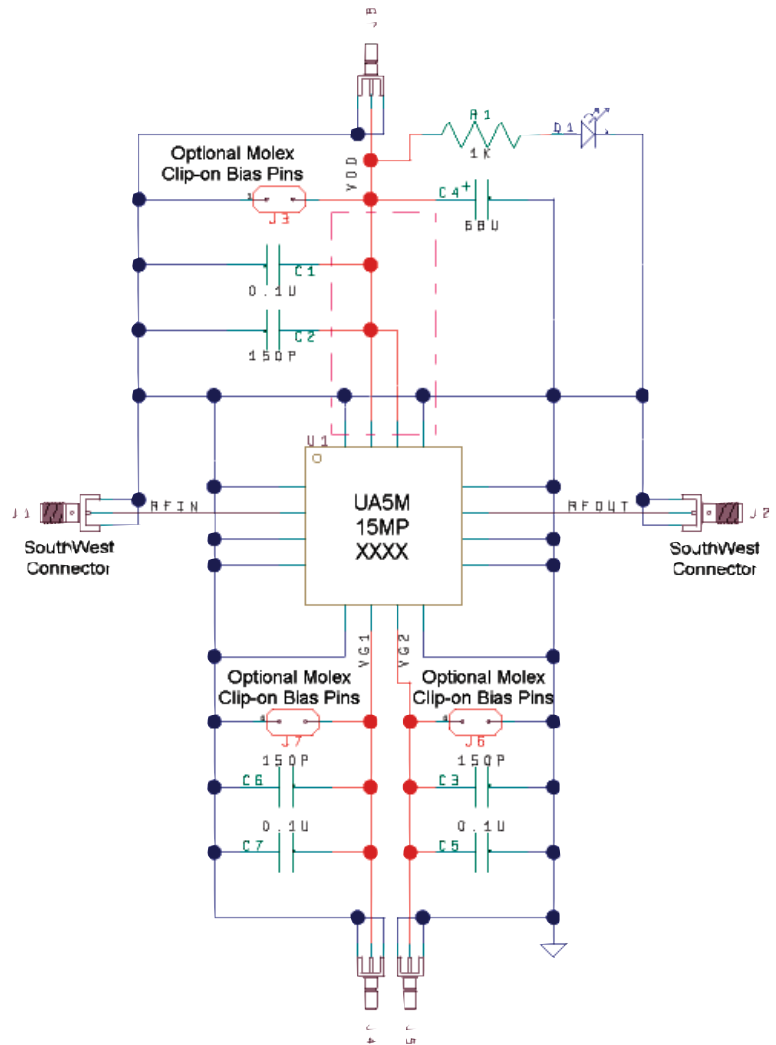


UA5M15MPE Evaluation Board



Evaluation Board Design Notes

1. UA5M15MP evaluation board is available upon request; part number is UA5M15MPE
2. PCB material is three-layer sandwich:
 - a. 8mil Rogers 4003; M1 above, M2 below
 - b. 39mil FR-4; M2 above, M3 below
 - c. 8mil Rogers 4003; M3 above, M4 below
3. SouthWest 2.92mm end-launch connectors are optimal for good performance
4. Follow Connector Attach Details for M2 ground plane cutaway under connector pin launch
5. 50Ω M1 GCPW line: W=14mil, S=4mil
6. M1 ground for CPW line is connected to M2 ground with a row of vias alongside the transmission line; see QFN Land Details
7. All QFN GND pads are connected to M1 ground and M2 ground (with vias)
8. PCB has solder mask to define pad locations
9. Solder paste and flux are screen-printed onto PCB for reflow attachment of QFN
10. PCB design recommendations and support is available from support@centellax.com



Evaluation Board Application Notes

1. Connect RFIN and RFOUT to 50Ω measurement system (connectors are SouthWest 2.92mm K-connectors, compatible with SMA)
2. Apply +3.3V or +5.0V drain bias voltage to VD1 and VD2 through the single SMB connector at the top of the board, or by connecting to the J3 Molex clip-on bias pins (see schematic)
3. Optionally connect 1st and/or 2nd stage gate bias voltages to VG1 and/or VG2 through the double SMB connectors at the bottom of the board, or by connecting to the Molex clip-on bias pins
4. Optionally adjust VG1 and/or VG2 for optimal application-specific performance