

## 39.8 - 56Gb/s PRBS SOURCE



### Features

- Self-contained PRBS Generator
- Built-in, quarter-rate clock source (14.0GHz)
- 1010, 1100, and 2e15 patterns
- 800-1600mV, adjustable differential output
- Quarter rate (Clk/4) clock input
- Quarter and half rate clock outputs
- Pattern trigger output

### Description

The Centellax 39.8-56Gb/s PRBS Source is a fully self-contained 56Gb/s pattern generator. This product has been designed to provide an excellent quality "EYE" at a fraction of the price of current market solutions. This is made possible through comprehensive integration of the key building blocks into monolithic integrated circuits founded on SiGe technology. The performance generated from the 39.8-56Gb/s PRBS Source is world class with the typical EYE having 400 fs rms jitter, 400 mV of output swing and <9 ps rise time.

All of this comes in a package one sixth the size of any other solution on the market which allows you to put your source directly at your device under test regardless of your lab bench environment.

### Application

The Centellax TG2P5A is designed to be used as the source for testing new 100 Gigabit Ethernet applications designed at one half data rate or 56Gbps. The TG2P5A, in conjunction with a high speed Digital Communications Analyzer can be used to make EYE and jitter measurements of 56Gbps components such as modulator drivers, optical modulators, MUX, and DEMUX components. The square wave patterns are ideal for separating data dependent jitter from random jitter for system jitter characterization. The superior rise time, fall time, and excellent jitter of the TG2P5A make it desirable for production component test where the source performance needs to be as good as possible to meet production specification margins. The low price of the TG2P5A make it desirable for manufacturing environments which are cost sensitive. The TG2P5A comes with an internal fixed 56G clock source or it can be used with an external clock source for other data rates in the 39.8-56Gb/s range.

# TG2P5A Datasheet



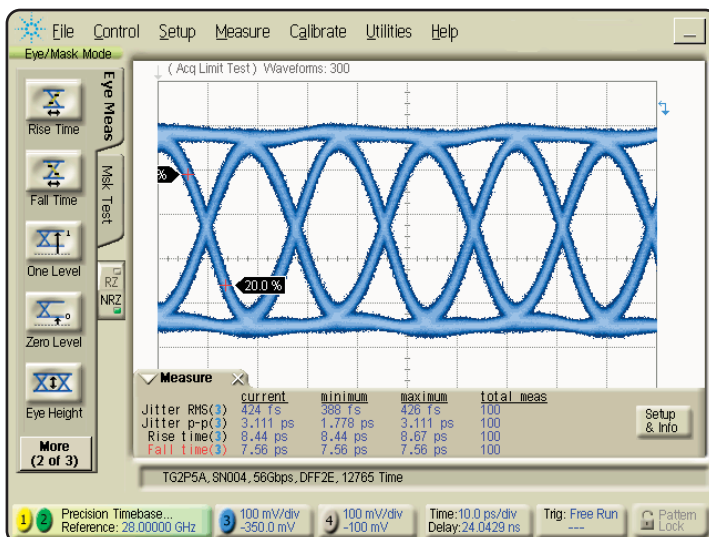
FRONT OF TG2P5A

| Label          | Description                                         |
|----------------|-----------------------------------------------------|
| Data Out ±     | Data Outputs<br>1.85mm F (V) connectors             |
| Data Amplitude | Data Output Amplitude Level<br>2:1 (6dB) range      |
| Clk2 Output    | Half-rate Clock Output<br>2.92mm F (V) connector    |
| Pattern Select | Pattern select switch<br>LEDs indicate state        |
| Clk2 Phase Adj | Half rate clock-2-data align<br>Adjust for best EYE |

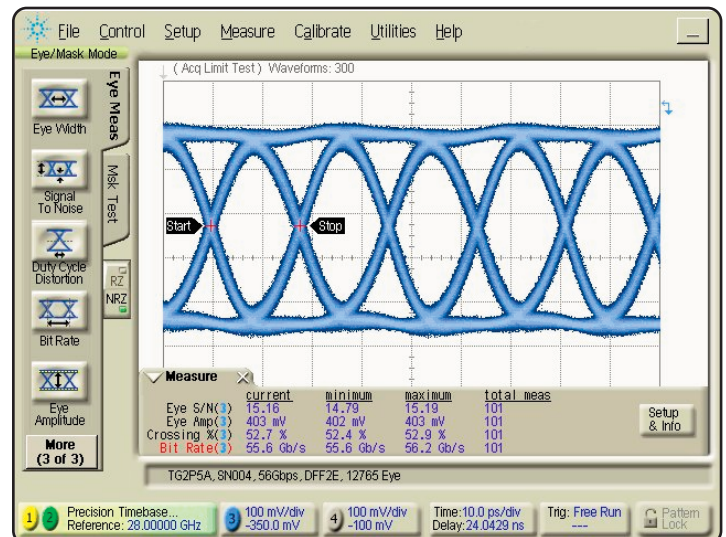


BACK OF TG2P5A

| Label           | Description                                                           | Label        | Description                                                                  |
|-----------------|-----------------------------------------------------------------------|--------------|------------------------------------------------------------------------------|
| Power           | Power Switch on/off<br>DC plug, 2.1 mm                                | Clk/4 In     | Main quarter rate clock input<br>Clk_rate = Bit_rate/4                       |
| Mux4 Clk Phase  | 4:1 Mux clock-2-data alignment<br>Adj for error-free operation        | Clk/4 Buf    | Buffered quarter rate clock output<br>Clk/4 Buf freq = Clk/4 freq            |
| DCD Bias Adjust | Adjacent EYE width adjustment<br>Adj (if req.) for equal EYE symmetry | Pattern Trig | Pattern Trigger<br>Square Wave, freq = $\frac{\text{Bit rate}}{(2e15-1)/32}$ |
| Clk/4 Out       | Built in clock output<br>Fixed 14.000 GHz frequency                   |              |                                                                              |



Time Parameters



Amplitude Parameters

## Performance Specification Table

| Parameter                        | Specifications |         |         | Units |
|----------------------------------|----------------|---------|---------|-------|
|                                  | Min            | Typ     | Max     |       |
| <b>Data Outputs</b>              | Min            | Typ     | Max     | Units |
| Bit Rate                         | 39.8           | 56.0    | 56.0    | Gb/s  |
| Amplitude (single-ended)         | 400            | -       | 800     | mV    |
| Rise/Fall Times (20-80%)         | -              | 7       | 8.0     | ps    |
| Rise/Fall Times (10-90%)         | -              | 10      | 11.5    | ps    |
| Jitter (RMS/PPK)                 | -/-            | 450/3.0 | 500/4.0 | fs/ps |
| <b>(Internal) Clock/4 Output</b> | Min            | Typ     | Max     | Units |
| Frequency (1/4 of bit rate)      | -              | 14.000  | -       | GHz   |
| Frequency Stability              | -              | -       | +/-20   | ppm   |
| Amplitude (single-ended)         | 1.0            | 1.7     | 2.2     | Vppk  |
| Duty Cycle                       | 48             | -       | 52      | %     |
| <b>Clock/4 Output</b>            | Min            | Typ     | Max     | Units |
| Frequency                        | 9.9            | -       | 14.0    | GHz   |
| Input Amplitude                  | 1.0            | 1.5     | 3.5     | Vppk  |
| Duty Cycle                       | 45             | 50      | 55      | %     |
| <b>(Buffered) Clock/4 Output</b> | Min            | Typ     | Max     | Units |
| Amplitude                        | 1.0            | 1.5     | 2.0     | Vppk  |
| Duty Cycle                       | 48             | -       | 52      | %     |
| <b>(Doubled) Clock/2 Output</b>  | Min            | Typ     | Max     | Units |
| Amplitude                        | 1.0            | 1.7     | 2.0     | Vppk  |
| Duty Cycle                       | 48             | -       | 52      | %     |